YM3434

(AFUDF)

2-Channel 8-times Oversampling Digital Filter

Operable at an independent system clock cycle from the input serial signal

■ OUTLINE

The digital filter's own system clock rate must be considerably faster than the input bit clock rate and at the same time synchronism is required in the system as a whole. Thus what is normally required is a high-speed clock which is synchronous with the signal handling pre-processor. Then the major application problem is how to interface these different clock rates.

YM3434 is a high quality 2-channel 8-times oversampling digital filter which has been developed to solve such problems. It can be used easily as an interface in a wide range of digital audio systems. Its filtering capabilities are equivalent to the YM3414.

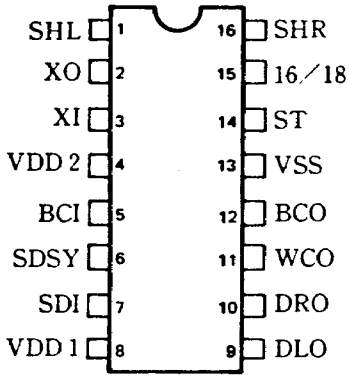
Since the system clock of this LSI can be different from the serial input signal and it operates normally at any clock rate above 400 clocks for each input sampling frequency (Fs), it is not necessary to change the clock rate even if the sampling frequency is changed.

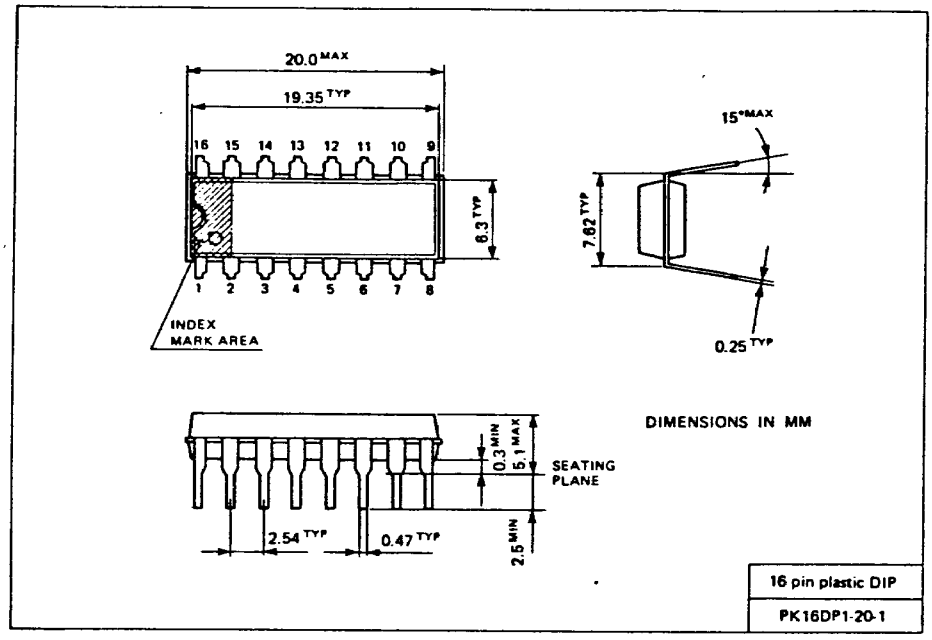
For example, by connecting a 20MHz crystal oscillator, there is no need to change the clock rate even when the sampling frequency is changed to 32KHz, 44.1KHz or 48KHz.

■ FEATURES

- Operation at an independent system clock from the serial input signal
- Input signals can be handled at any of the following input bit clock rates without adding any circuit: 32Fs, 48Fs, 64Fs, 80Fs, 96Fs, 112Fs, 128Fs, 144Fs, 160Fs, 176Fs and 192Fs.
- Capable to cope with sampling frequencies 32KHz, 44.1KHz and 48KHz.
- Linear phase FIR type filters connected in three vertical stages
  1st filter : 225-order FIR filter
  2nd filter : 41-order FIR filter
  3rd filter : 21-order FIR filter
- Built-in 19 × 18 bit multiplier, floating point calculation with a coefficient of 18 bits
- Built-in overflow limiter
- Filter characteristics (at 8-times)
  Pass band ripple : Within ±0.0001dB at 0 to 0.4535 × Fs
  Stop band attenuation : At least 100dB at 0.5465 × Fs to 7.4535 × Fs
- Output data switchable between 16 bit and 18 bit (directly connectable to BB Corporation's PCM56 and PCM58).
- Switchable between 1 DAC (4-times) and 2 DAC (8-times).
- C-MOS type processor, Single 5 V power supply, 16-pin type DIP package.

■ TERMINAL DIAGRAM ■ TERMINAL FUNCTIONS

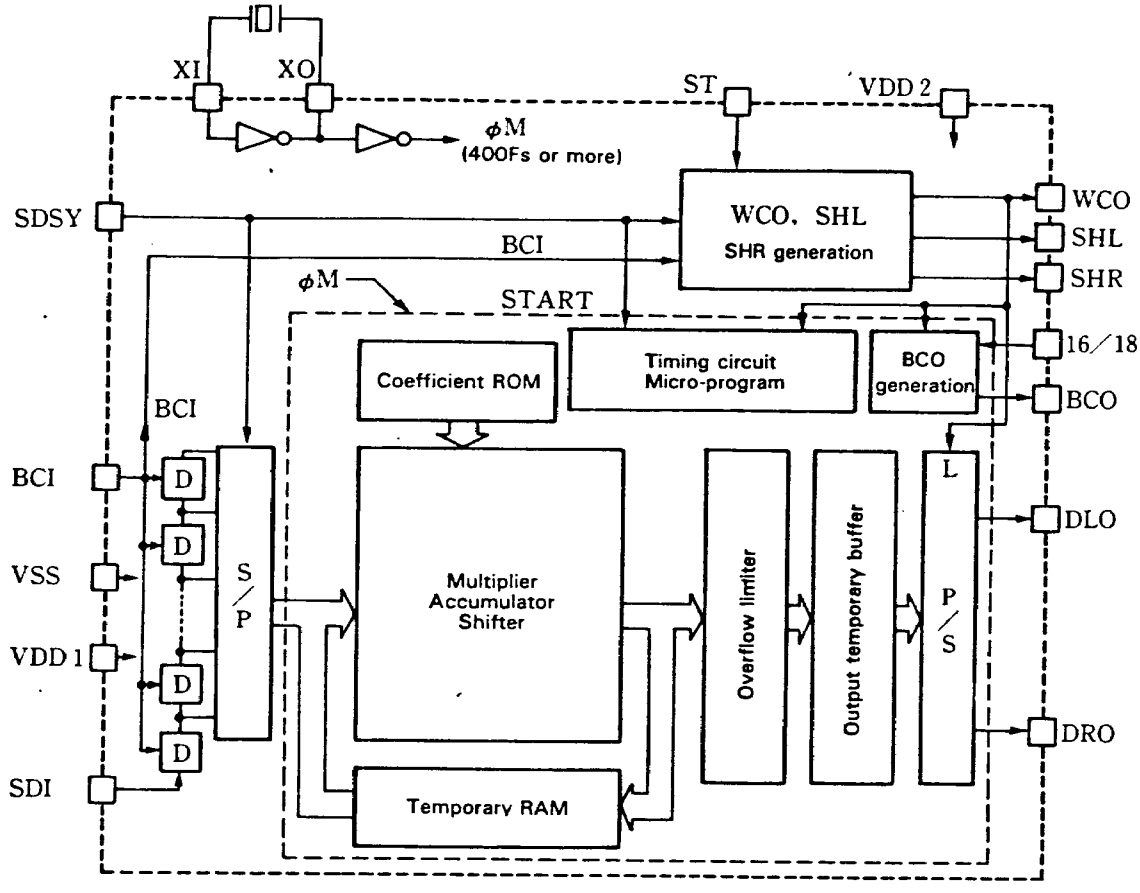




■ EXTERNAL DIMENSIONS

Terminal Name	Pin No.	I/O	Outline of Function
SHL	1	O	Lch degricher signal at 1 DAC (ST="L") L/Rch degricher signal at 2 DAC's (ST="H")
XO XI	2 3	O I	System clock crystal oscillation between XI and XO Clock rate can be input directly to SI
VDD 2	4	—	+5V power supply terminal for crystal oscillation and degricher signal.
BCI	5	I	Bit clock input terminal for input data
SDSY	6	I	Clock input terminal for indicating Lch or Rch and input timing.
SDI	7	I	Data input terminal
VDD 1	8	—	+5V power supply terminal
DLO	9	O	Lch and Rch data output terminal at 1 DAC (ST="L") Lch data output terminal at 2 DAC's (ST="H")
DRO	10	O	Rch data output terminal
WCO	11	O	Word clock output terminal for output data DLO and DRO
BCO	12	O	Bit clock output terminal for output data DLO and DRO
VSS	13	—	Ground terminal
ST	14	I	1 DAC/2 DAC's switching terminal (1 DAC="L", 2 DAC's="H")
16/18	15	I	Output data bit number switching terminal (16 bit="L", 18 bit="H")
SHR	16	O	Rch degricher signal at 1 DAC (ST="L")

■ Block Diagram



■ Outline of Functions

• Timing functions

- The digital data signal input through the SDI pin is set on the S/P (Serial/Parallel) converter by the BCI and SDSY synchronous signals.
- The Word Clock Output (WCO) and degricher signals (SHL and SHR) are generated by counting the Bit clock input (BCI) in one word clock input (SDSY) cycle.
  If the BCI count in one SDSY cycle is a multiple of 16 and between 32 Fs and 192 Fs, WCO, SHL and SHR signals with a jitter grade equivalent to the BCI's one can be generated at any rate. However, it should be noted that if there is a change in the duty value of the input BCI data, that change will also appear in WCO, SHL and SHR signals.
- The digital filtering section operates at the clock rate input through the XI pin. The calculation operation begins at the XI timing immediately after a change in SDSY and the caluculated result is stored in the output temporary buffer. The digital filter enters the wait status after the calculation and remains in this state until the SDSY value changes, which means that it operates at the same XI clock even when the SDSY (sampling) cycle changes. The XI clock for one SDSY cycle must be at least 400 Fs and any value beyond that will only affect the wait time. As the data output to DLO and DRO is started at the timing as calculated on the SDSY and BCI inputs and done at half the XI clock rate, enough time is available for the digital-analog converter to operate.
- As a result, this LSI can be used as a high performance digital filter interface without connecting the signal processing section before this LSI and the synchronous high speed clock and without changing the XI clock by means of the sampling frequency.
- The functions of the digital filter are obtained by connecting the linear phase 225th FIR type filter as the first filter, the linear phase 41st FIR type filter as the second one and the linear phase 21st FIR type filter as the third one in the three vertical stages.
  The internal multiplier has a 19 by 18 bit structure with a built-in overflow limiter and uses the 18 bit floating point calculation system.

- Any of the following input data can be processed as long as it is a 16 bit 2-channel MSB first data: 32Fs, 48Fs, 64Fs, 80Fs, 96Fs, 112Fs, 144Fs, 160Fs, 176Fs and 192Fs.
- The output data can be obtained in the signal format of 8-times 2 DAC or 4-times 1 DAC by using the switching function of ST pin. As the output data is also switchable between the 16-bit and 18-bit output by using the switching function of 16/18 pin, it is possible to connect BB Corporation's PCM56 (16 bit) and PCM58 (18 bit) directly to this unit.

Filter Characteristics (theoretical values)	At 8-times (2 DAC) :	At 4-times (1-DAC)
Pass band characteristics :		
Pass band ..... 0 ~ 0.4535 × Fs	:	0 ~ 0.4535 × Fs
Pass band ripple..... Within ±0.0001 dB	:	Within ±0.0001 dB
Stop band characteristics :		
Stop band ..... 0.5465 × Fs ~ 7.4535 × Fs	:	0.5465 × Fs ~ 3.4535 × FS
Stop band attenuation .... Over −100 dB	:	Over −100 dB
Slope characteristics :		
−0.00016 dB (At frequency=0.4535 × Fs)	:	−0.00013 dB (At frequency=0.4535 × Fs)
−104 dB (At frequency=0.5465 × Fs)	:	−102 dB (At frequency=0.5465 × Fs)

■ Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	VI	−0.3	V_{DD}+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

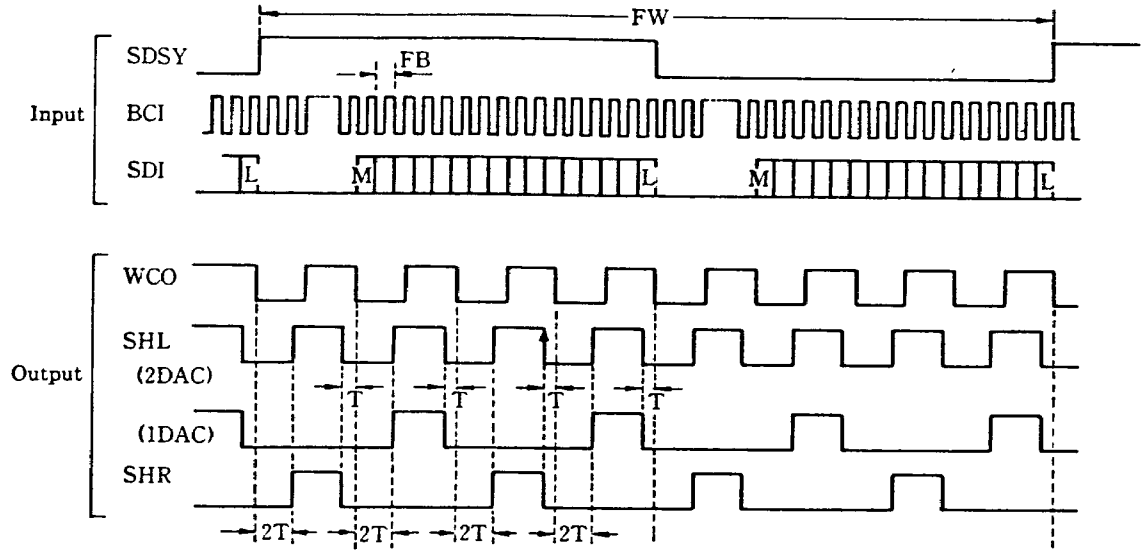
■ Recommended Working Conditions

Item	Symbol	Minimum	Standard	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Clock frequency	XIN	12.2	(400 Fs)	20.0	MHz
Working temperature	Top	0	25	+70	°C

■ Electrical Characteristics

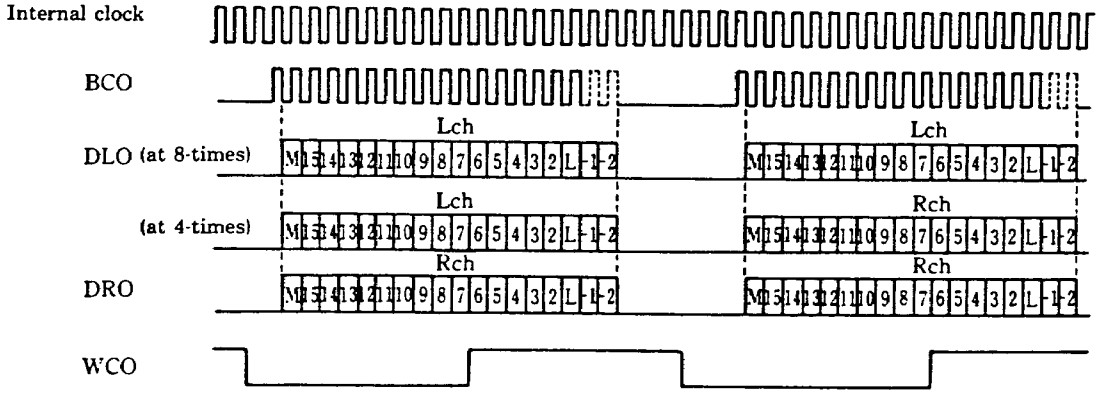
Item	Symbol	Conditions	Minimum	Standard	Maximum	Unit
Power consumption	W	V_{DD}=+5V			300	mW
Input voltage H level (XI, 16/18, ST) (BCI, SDSY, SDI)	VIH		 3.5 2.7		 V_{DD} V_{DD}	 V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		V_{DD}	V
Output voltage L Level	VOL		0		0.4	V
DLO, DRO setup time DLO, DRO hold time			15 15			ns ns
Input data setup time (Rise of BCI)			50			ns
Input data hold time (Rise of BCI)			20			ns
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ Serial Input Timing and WCO, SHL, SHR Output Timing



- T and 2T values at various input frequencies are as follows:
  At 32Fs : T=FB/2, 2T=FB (FB represents the input bit clock)
  At 48Fs to 112Fs : T=FB, 2T=2×FB
  At 128Fs or higher : T=2×FB, 2T=4×FB
- The FB cycle within the FW period must be greater than 32 and less than 2 and must be a multiple of 16, 32, 48, 64, 80, 96, 112, 128, 144, 160, 176 and 192
- SDSY, BCI and SDI input signals must be synchronous and then WCO, SHL and SHR output signals will be synchronous. However, the former and latter signals need not be synchronous.

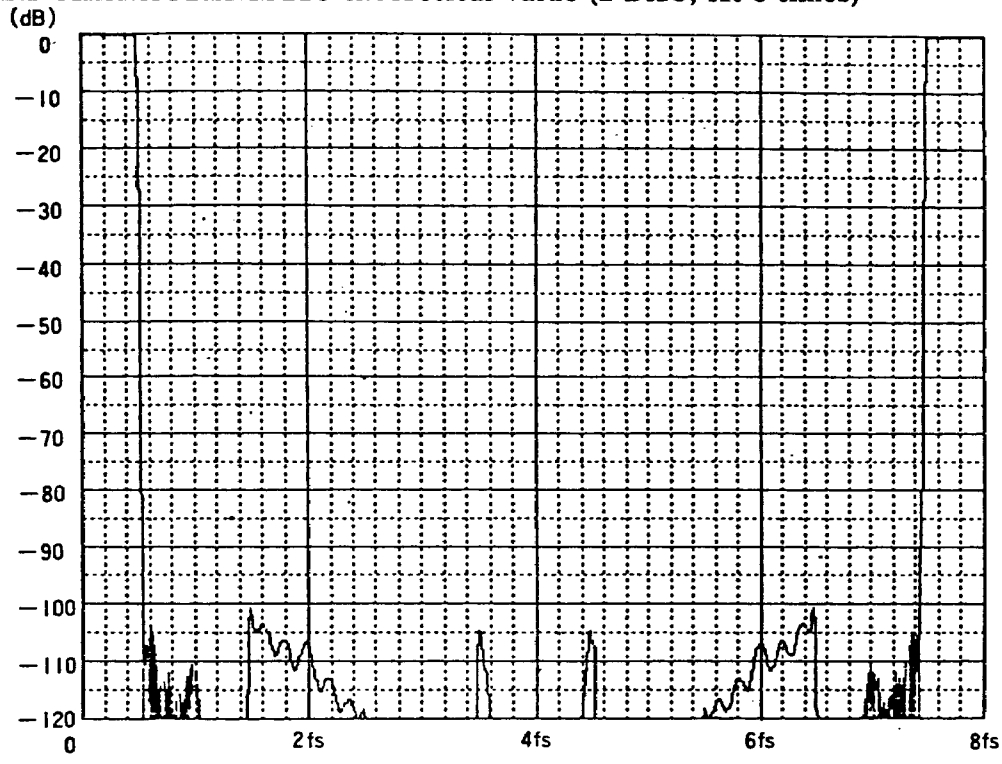
■ BCO, DLO, DRO, WCO Output Timing



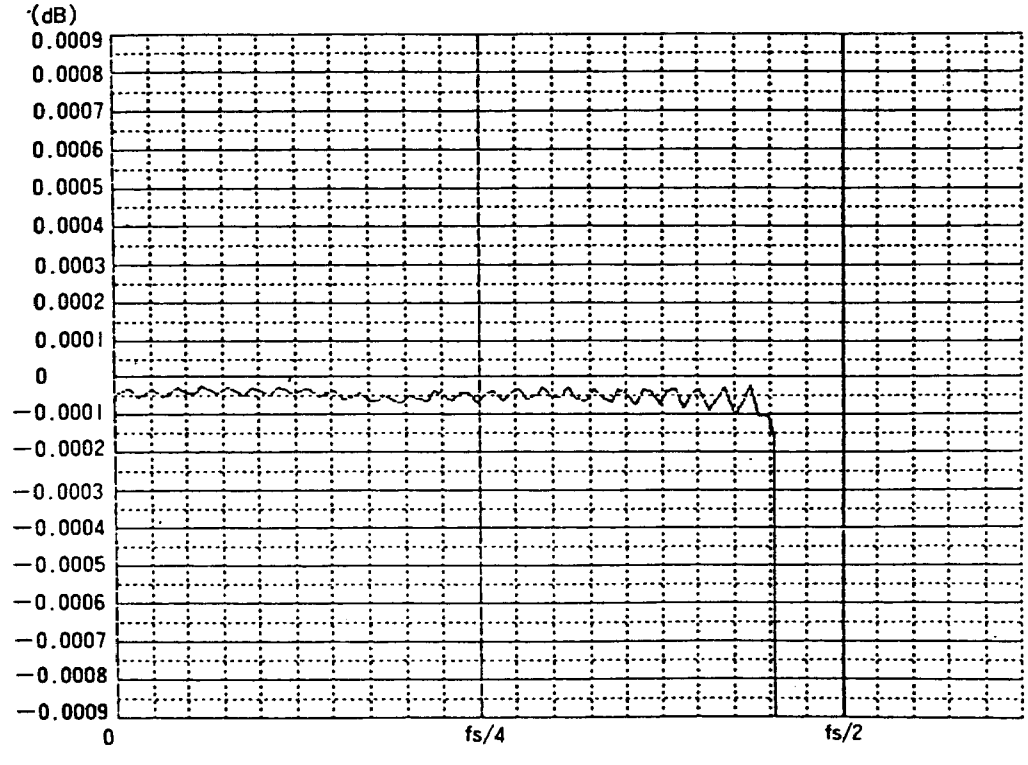
- BCO, DLO and DRO signals are synchronous but they are not synchronous with the WCO signal.
- The BCO clock rate is the rate when the XI input clock is divided by 2.
- The broken line part of the BCO signal shows the BCO clock at 18 bit output (16/18 terminal = "H").
- −1 and −2 values in the DLO and DRO signals correspond to the output at the 17th and 18th bit respectively.
- The WCO fall occurs only when the BCO is inactive.

■ CHARACTERISTICS FOR REFERENCE

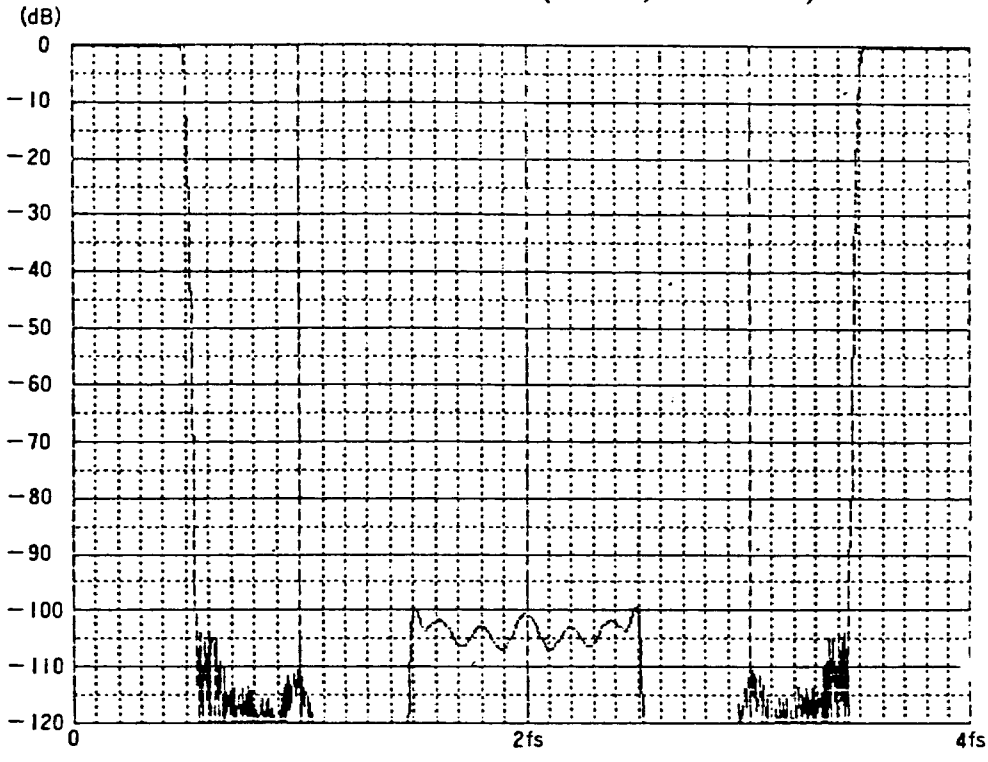
OVERALL CHARACTERISTIC theoretical value (2 DAC, At 8-times)



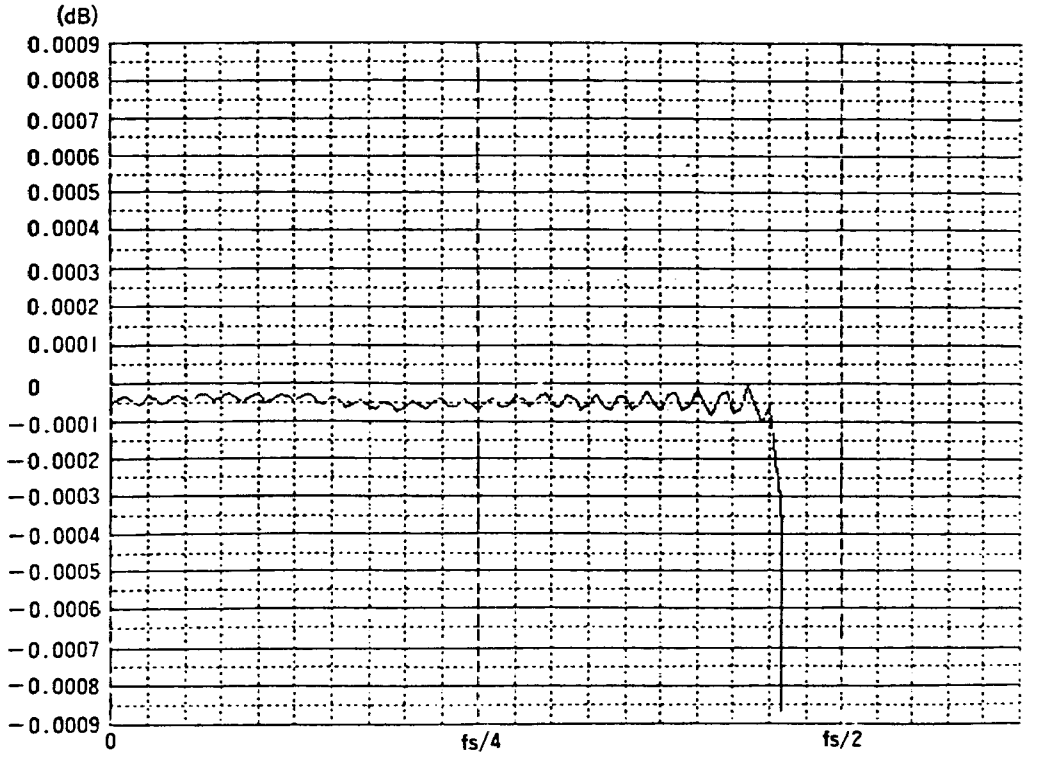
OVERALL PASS BAND CHARACTERISTIC theoretical value (2 DAC, At 8-times)



OVERALL CHARACTERISTIC theoretical value (1 DAC, At 4-times)

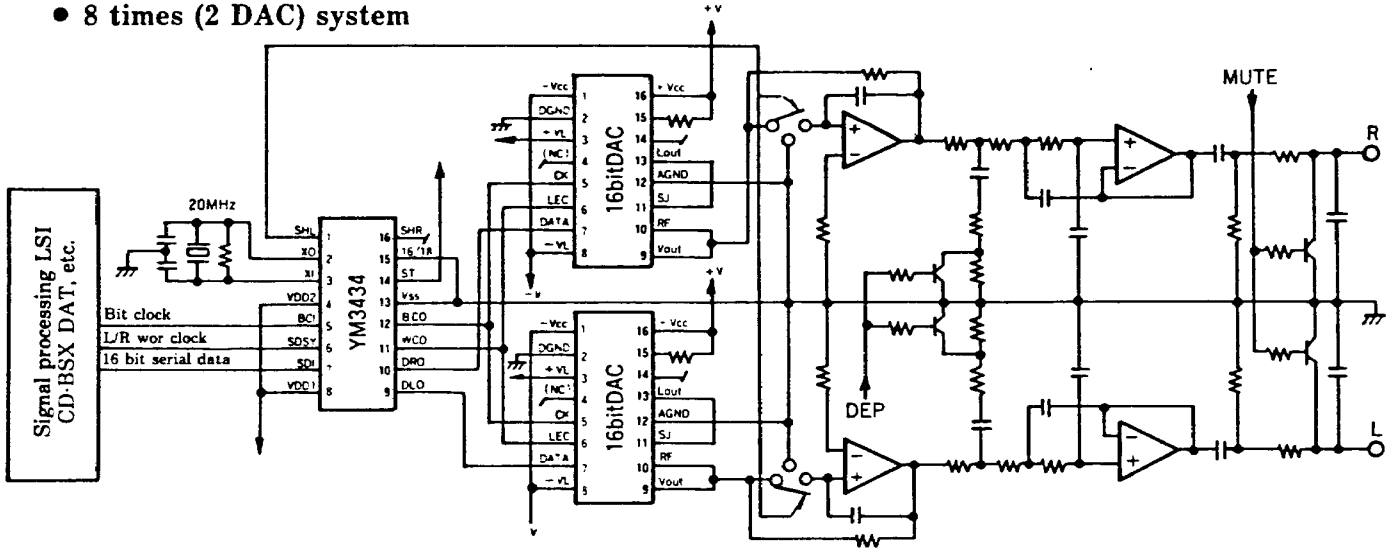


OVERALL PASS BAND CHARACTERISTIC theoretical value (1 DAC, At 4-times)

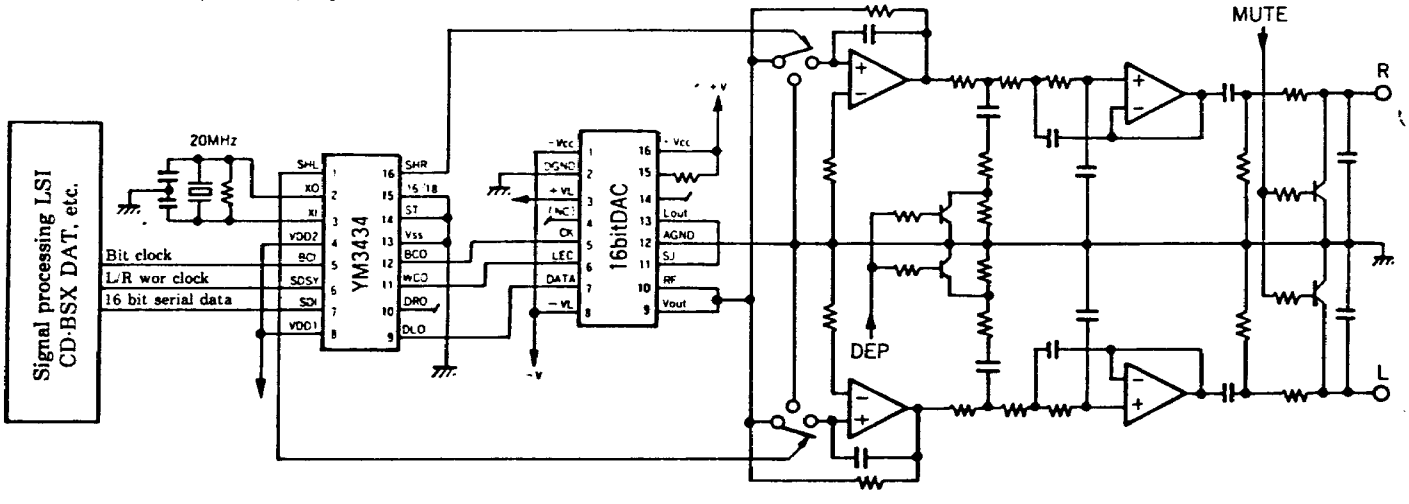


■ Application Samples

• 8 times (2 DAC) system



• 4 times (1 DAC) system



The specifications of this product are subject to improvement changes without prior notice.

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