NO. 85-10

# YM3020

## 2-Channel Serial & Binary input Floating D/A Converter(DAC-FS)

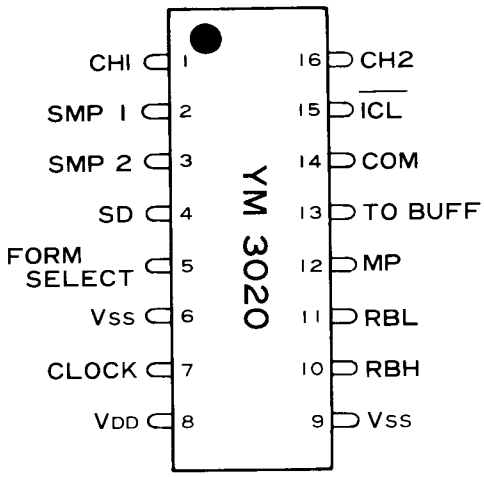
## ■ OUTLINE

The YM 3020: DAC-FS is a floating D/A converter (referred to as DAC hereafter) with the 2-channel serial and 16-bit binary input or 2's complement input. It can produce analog output (16-bit dynamic range) which has 13-bit mantissa and 7-step exponent characteristic for the input digital signal.

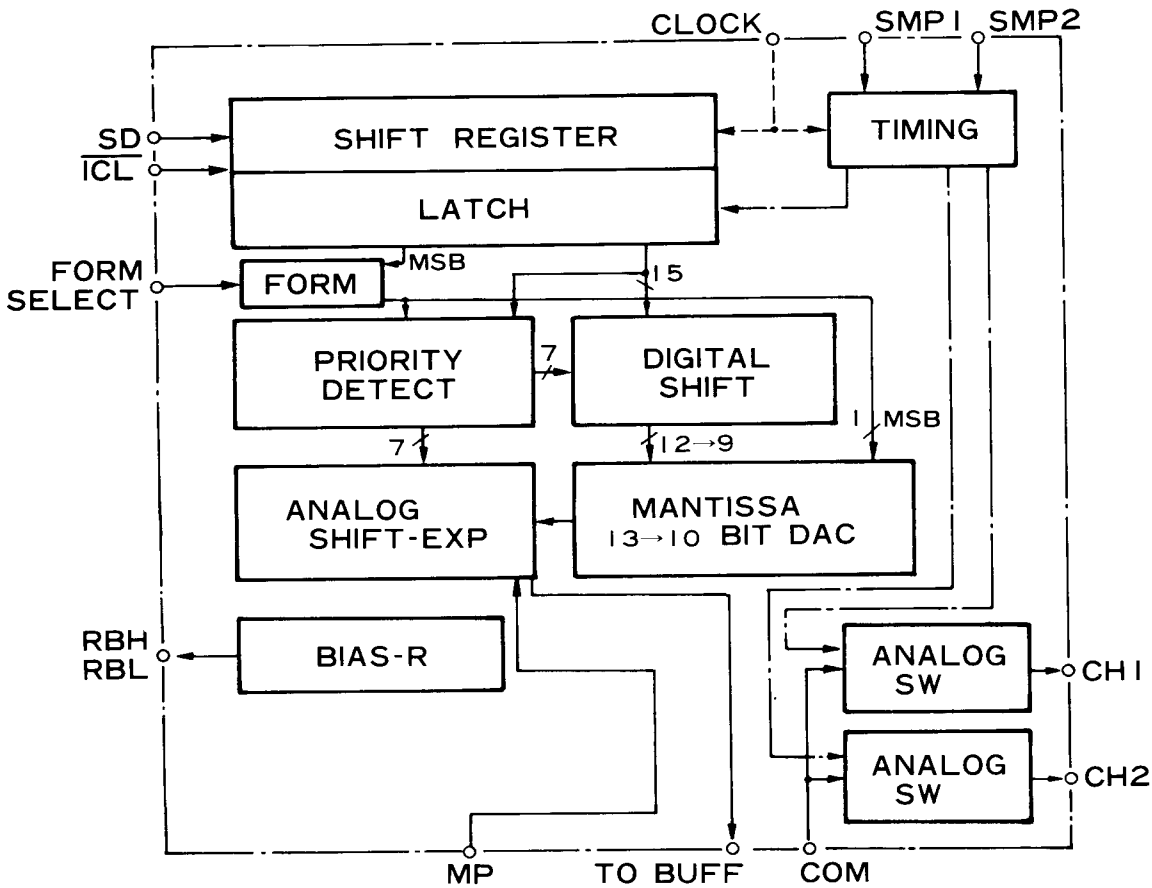
## ■ FEATURES

- 16-bit input format can select either binary or 2's complement (equipped with a built-in floating converter logic).
- Externally equipped with buffer operational amplifier it allows easy analog output.
- 16-bit wide dynamic range.
- Capable of processing PCM sound source up to 2 channels.
- Equipped with a built-in analog switch for sample hold.
- Lower noise and less harmonic distortion and outstanding temperature characteristics. Zero cross distortion is extremely little.
- Made by the monolithic process of highly accurate thin film resistance and CMOS and enclosed in the 16-pin plastic DIL package.

## ■ Pin assignment




## ■ Block diagram



## ■Pin function

| Pin No. | Signature | Description |
|---|---|---|
| 1 | VOUT CH1 | Sample hold analog switch output for CH1 |
| 2 | SMP1 | Interval "1" becomes sampling time for CH1. |
| 3 | SMP2 | Interval "1" becomes sampling time for CH2.<br>The internal signal for latching serial data is produced by using SMP1 and SMP2 fall. The longer the SMP1 and SMP2 time is, the more improved the level frequency response is. |
| 4 | SD | Serial input of digital signal to be converted |
| 5 | FORM SELECT | Capable of processing binary input format at "1" and 2's complement input format at "0". |
| 6 | VSS | Low electric potential side power source (GND) |
| 7 | CLOCK | Clock to operate shift register and timing generator (∅4) |
| 8 | VDD | High electric potential side standard power source |
| 9 | VSS | Low electric potential side standard power source (GND) |
| 10 | RBH | As the same resistor is used between the RBH pin and internal VDD power source and between the RBL pin and internal VSS (GND) power source, connecting both pins will provide highly accurate 1/2 VDD voltage. The voltage is applied to the MP pin through the buffer operational amplifier. |
| 11 | RBL | As shown in the standard circuit example, deviation from the 1/2 VDD can be corrected by adding a suitable resister externally. |
| 12 | MP | Exponential analog shift is carried out with the electric potential applied to the MP as a standard. Normally it is biased to the 1/2 VDD. |
| 13 | TO BUFF | DAC analog output, input to the buffer operational amplifier |
| 14 | COM | Common input to analog switches for CH1 and CH2 |
| 15 | $\overline{ICL}$ | The signal "1" - normal operation and "0" - zero signal operation regardless of the signal SD. |
| 16 | VOUT CH2 | Sample hold analog switch output for CH2 |

## ■ Description of Operation

### 1. Operation

The serial digital input data is synchronized with the clock fall and taken into the shift register through the SD pin. The latch signal is produced in the timing circuit by making use of the fall of SMP1 and SMP2 and it latches $I_{15} \sim I_0$ serial data.

After being latched, the 16-bit binary or 2's complement input data or $I_{15}$ to $I_0$ are logic converted into the data for the floating DAC by means of the priority detecting circuit and digital shift circuit. Then they become 13 → 10 bit mantissa DAC data and 7-step exponential characteristic DAC (analog shift) data and determine the DA conversion output value.

The data conversion truth table is given below.

| | Analog shift | | | | | | |
|---|---|---|---|---|---|---|---|
| N | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
| 「1」 | $S_0$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
| $I_{14}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $I_{13}$ | | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $I_{12}$ | | | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $I_{11}$ | | | | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $I_{10}$ | | | | | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $I_9$ | | | | | | $I_{15}$ | $I_{15}$ |

This is the case of 2's complement input. With binary input, positive and negative of $I_{15}$ are reversed.

| Mantissa 13 bit data | Analog shift | | | | | | |
|---|---|---|---|---|---|---|---|
| | 「1」 | $S_0$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
| $D_{12}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ | $I_{15}$ |
| $D_{11}$ | $I_{14}$ | $I_{13}$ | $I_{12}$ | $I_{11}$ | $I_{10}$ | $I_9$ | $I_8$ |
| $D_{10}$ | $I_{13}$ | $I_{12}$ | $I_{11}$ | $I_{10}$ | $I_9$ | $I_8$ | $I_7$ |
| $D_9$ | $I_{12}$ | $I_{11}$ | $I_{10}$ | $I_9$ | $I_8$ | $I_7$ | $I_6$ |
| $D_8$ | $I_{11}$ | $I_{10}$ | $I_9$ | $I_8$ | $I_7$ | $I_6$ | $I_5$ |
| $D_7$ | $I_{10}$ | $I_9$ | $I_8$ | $I_7$ | $I_6$ | $I_5$ | $I_4$ |
| $D_6$ | $I_9$ | $I_8$ | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ |
| $D_5$ | $I_8$ | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ |
| $D_4$ | $I_7$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ |
| $D_3$ | $I_6$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |
| $D_2$ | $I_5$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $V_M$ |
| $D_1$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $V_M$ | $V_M$ |
| $D_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $V_M$ | $V_M$ | $V_M$ |

*$V_M$: Terminated at the 1/2 $V_{DD}$ midpoint electric potential.

The DA converted analog output voltage is, for example with the standard circuit, as follows.

$$V_{OUT} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD}(-1 + D_{12} + D_{11}2^{-1} + \cdots\cdots + D_0 2^{-12} + 2^{-13})\,2^{-N}$$

It has 1/2 $V_{DD}$ maximum amplitude and 1/2 $V_{DD} \cdot 2^{-16}$ minimum amplitude with the 1/2 $V_{DD}$ electric potential as the center.

The analog output comes out to the TO BUFF pin. When this is input through an appropriate buffer operational amplifier and resistor into the COM pin, it is output to the CH1 and CH2 pins in the interval "1" of the SMP1 and SMP2, and the analog output of each channel is retained to the proper electrostatic capacity in the interval "0".

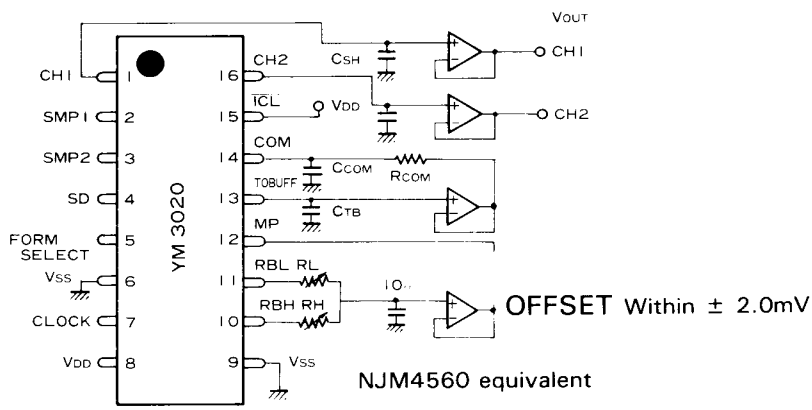
### 2. Tips on Operation

- As shown in the timing diagram Fig. 3, be sure to synchronize the fall of SMP1 and SMP2 with the rear end timing of the MSB ($I_{15}$) signal.
- The sampling time of the SMP1 and SMP2 can be set to other than 8-bit time which is shown in Fig. 3.
- When using the CH1 only, be sure to synchronize the rear end timing of the MSB ($I_{15}$) signal and the SMP1 fall timing, for example, by setting the SMP2 to $V_{SS}$.
- When executing the conversion cycle at a different bit time, an adjustment can be made by increasing or decreasing the number of invalid bits.

### 3. Initial Clear Function

Setting the $\overline{ICL}$ to "0" will clear the serial input data regardless of digital input data value and results in output without signal.

## ■ Standard circuit example




External constant example

| | | | | |
|---|---|---|---|---|
| Sample hold capacity | $C_{SH}$ | 1800PF ~ 3900PF | [2200PF] | recommended |
| Common resistor | $R_{COM}$ | 0 ~ 180Ω | [100Ω] | |
| Stabilized capacity | $C_{TB}$ | 68PF | | |
| | $C_{COM}$ | None | | |
| Midpoint correction resistance | RH | 0 ~ 70Ω | (It is recommended to adjust the MAX 100 to 200Ω variable resistor so as to minimize THD.) | |
| | RL | 0Ω | | |

For the $V_{DD}$ power source, it is desirable to use the one equivalent to the commercially available 3-pin regulator for the output impedance and stability.

## ■ Electrical Characteristics

### 1. Absolute maximum rating

| Item | Rating | Unit |
|---|---|---|
| Supply voltage | −0.3 ~ +15.0 | V |
| High-level input voltage | $V_{DD}$ +0.3 | V |
| Low-level input voltage | $V_{SS}$ −0.3 | V |
| Operating ambient temperature | 0 ~ 70 | °C |
| Storing temperature | −50 ~ +125 | °C |

### 2. Recommended operating conditions

| Item | Signature | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 9.0 | 12.0 | 12.0 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input signal voltage | CLOCK, SD, SMP1, 2, $\overline{ICL}$ | 0 | — | $V_{DD}$ | V |
| Operating ambient temperature | Ta | 0 | — | 70 | °C |

### 3. DC characteristics

| Item | Signature | Measuring Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{DD} \geqq 9.0V$ | 1/3 $V_{DD}$ | — | — | V |
| Low-level input voltage | $V_{IL}$ | $V_{DD} \geqq 9.0V$ | — | — | 1.0 | V |
| Input current | $I_{IN}$ | $V_{DD} = 12.0V$ | — | — | $10^{-3}$ | μA |
| Analog output voltage | $V_{OUT}$ | | — | 0.50$V_{DD}$ | — | Vp−p |
| Supply current | $I_{DD}$ | $V_{DD} = 12.0V$ | — | — | 6 | mA |

### 4. AC characteristics

| Item | Signature | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| • Clock | | | | | | |
| Frequency | fc | | 0.65 | 4.3 | 5.0 | MHz |
| High-level time | $T_H$ | | 100 | | | ns |
| Rise time | $T_r$ | | | | 30 | ns |
| Fall time | $T_f$ | | | | 30 | ns |
| • Data | | | | | | |
| Setup time | $T_{DS}$ | SD, SMP 1 | 50 | | | ns |
| Rise time | $T_r$ | SMP 2 | | | 30 | ns |
| Fall time | $T_f$ | | | | 30 | ns |

### 5. Capacity

| Item | Signature | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Input capacity | $C_{IN}$ | | — | — | 5 | PF |

## 6. DAC characteristics

| Item | Signature | Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum output amplitude | $V_{OUT}$ | | | 1/2 $V_{DD}$ | | $V_{pp}$ |
| Resolution | | | | 16 | | Bit |
| Settling time | $T_s$ | | | 2.0 | 3.5 | $\mu$sec |
| Total harmonic distortion * | THD 1 | $V_{DD}$ = 9V ~ 12.0V, 1KHz, | | | | |
| Noise contained | | Level 0dB | | 0.025 | 0.050 | % |
| | THD 6 | −40dB | | 0.17 | 0.35 | % |
| Noise | | | | −94 | −80 | dBm |
| Crosstalk | | 1KHz·0dB | | −80 | | dB |
| Temperature characteristics | | Output voltage | | | | |
| | | Total harmonic distortion | | 5 | | ppm/°C |

*Midpoint buffer operational amplifier NJM4560 (offset voltage within ±2.0mV) used, recommended constant used, especially $V_{DD}$ 12.0V recommended. Any other voltage is specified separately.

## 7. Timing Diagram

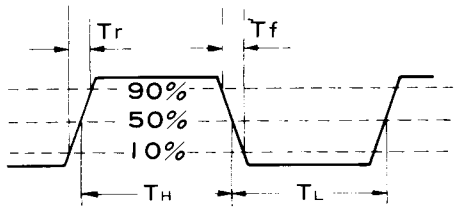



Fig. 1 Data timing

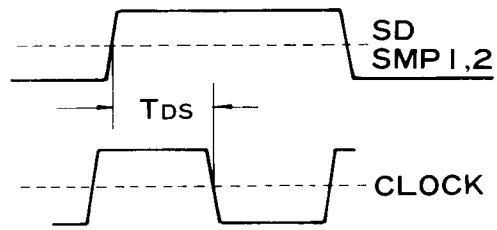



Fig. 2 Input data clock timing

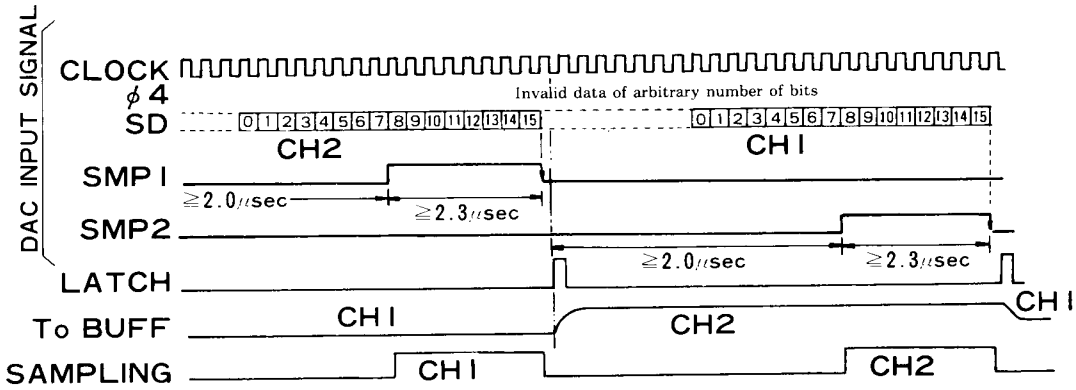
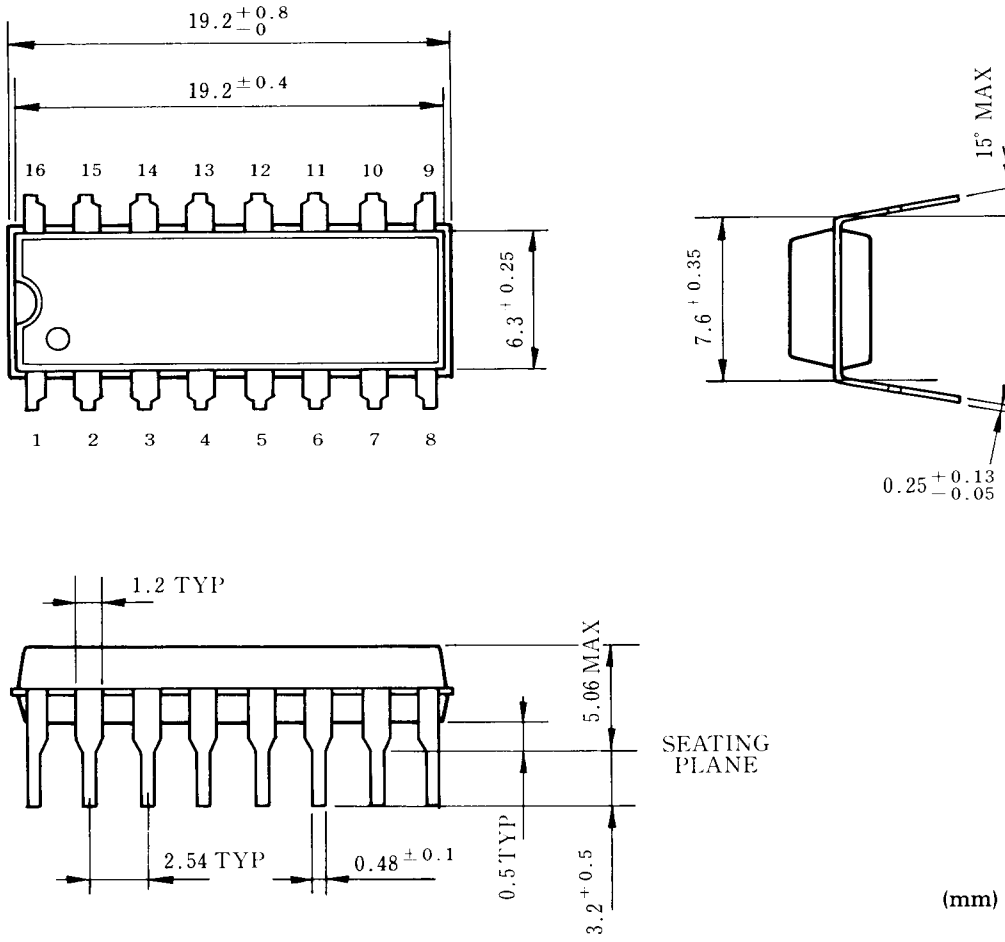



Fig.3 YM 3020 TIMING

## ■ Dimensions




*Specifications subject to change for improvement without notice.

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