

## 14-BIT DAC WITH 85 dB S/N RATIO

### GENERAL DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

### QUICK REFERENCE DATA

Supply voltages			
pin 4	V <sub>P1</sub>	typ.	5 V
pin 7	V <sub>N1</sub>	typ.	-5 V
pin 11	V <sub>N2</sub>	typ.	-17 V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85 dB
Non-linearity at T <sub>amb</sub> = -20 to + 70 °C		typ.	½ LSB
Current settling time	t <sub>cs</sub>	typ.	0,5 µs
Maximum input bit rate at data input (pin 1)	BR <sub>max</sub>	min.	12 Mbit/s
Maximum clock frequency at clock input (pin 28)	f <sub>cl max</sub>	min.	12 MHz
Full scale temperature coefficient at analogue output (pin 22)	TC <sub>FS</sub>	typ.	± 30 · 10 <sup>-6</sup> K <sup>-1</sup>
Operating ambient temperature range	T <sub>amb</sub>		-20 to + 70 °C
Total power dissipation	P <sub>tot</sub>	typ.	350 mW

### PACKAGE OUTLINE

TDA1540P: 28-lead DII · plastic (SOT-117).

**FUNCTIONAL DESCRIPTION**

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current  $4I$  of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents  $I$  ( $\bar{I}_1$ ),  $I$  ( $\bar{I}_2$ ) and  $2I$  ( $\bar{I}_3$ ) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be  $0\text{ V} \pm 10\text{ mV}$ . The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

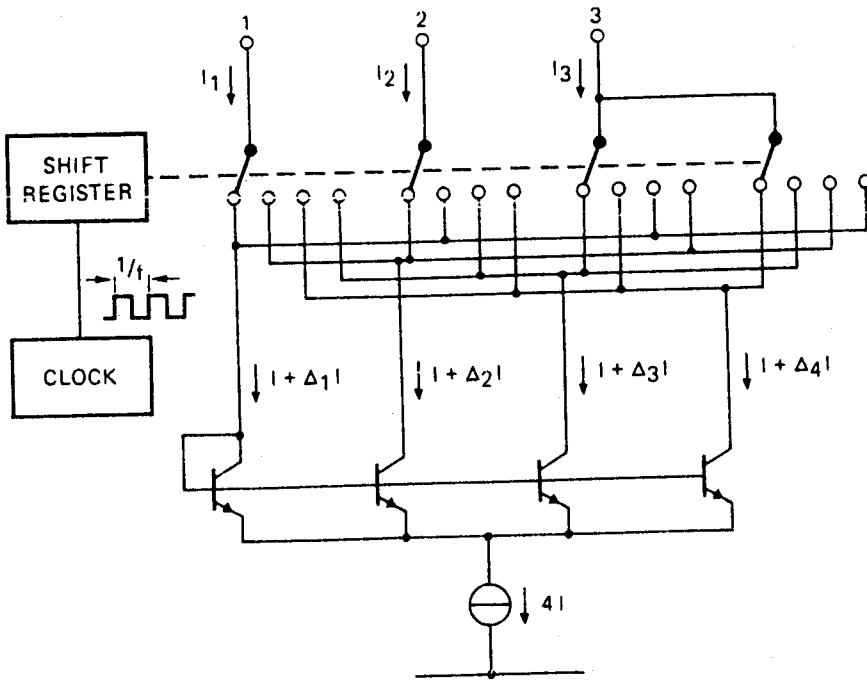


Fig. 1a Circuit diagram of one divider stage.

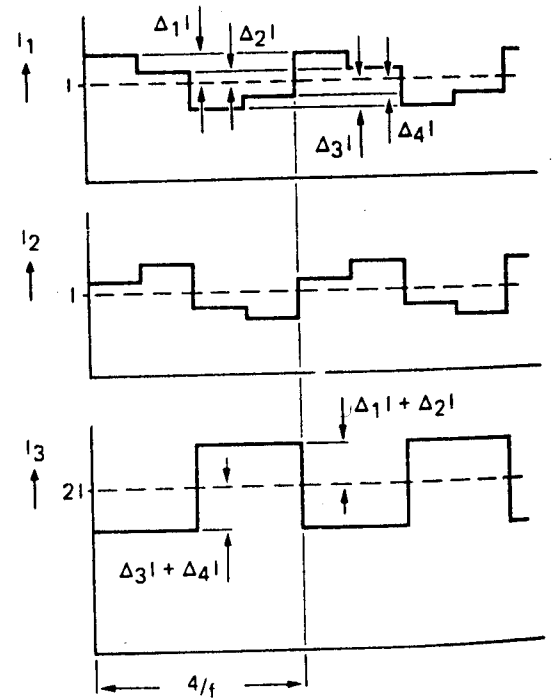
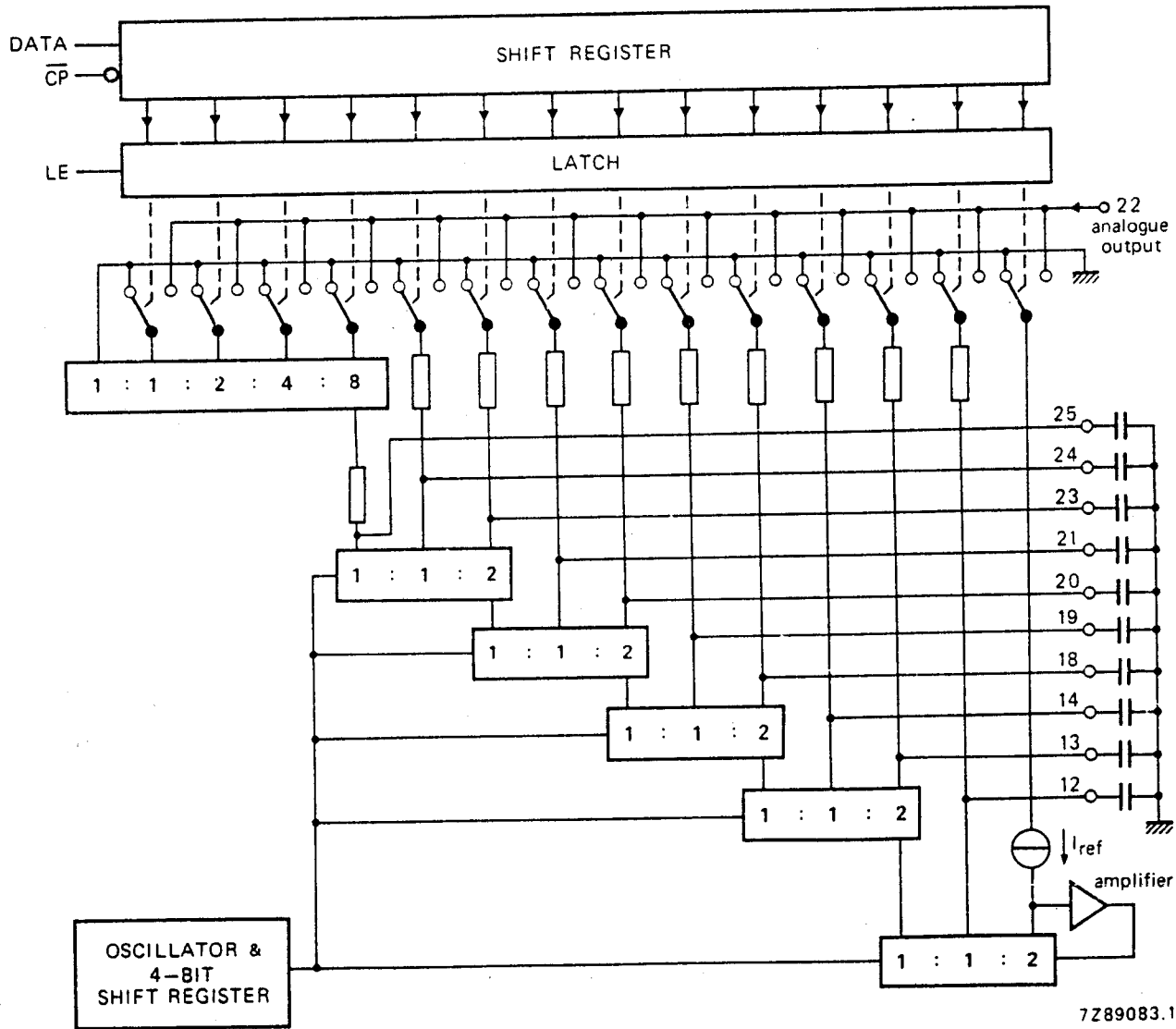


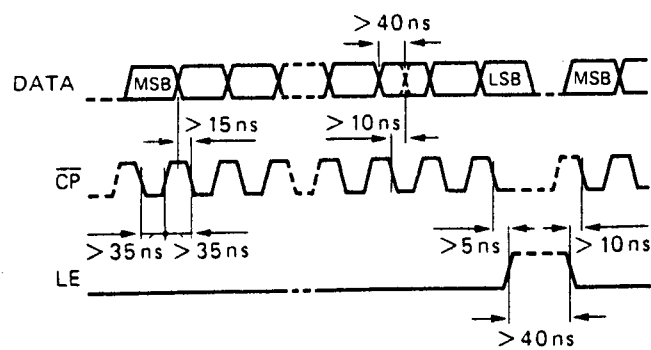
Fig. 1b Waveforms showing output currents  $I_1$ ,  $I_2$  and  $I_3$  of Fig. 1a.

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Fig. 2 Functional diagram showing cascading of current division stages.



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Fig. 3 Format of input signals.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

### Supply voltages

with respect to GND (pin 6)	$V_{P1}$	max.	12 V
at pin 4	$V_{N1}$	max.	-12 V
at pin 7	$V_{N2}$	max.	-20 V
at pin 11	$V_{P1}-V_{N2}$	max.	32 V
at pin 4 with respect to pin 11	$V_{N1}-V_{N2}$		-1 to +20 V
at pin 7 with respect to pin 11	$P_{tot}$	max.	600 mW
Total power dissipation	$T_{stg}$		-55 to +125 °C
Storage temperature range	$T_{amb}$		-25 to +80 °C
Operating ambient temperature range			

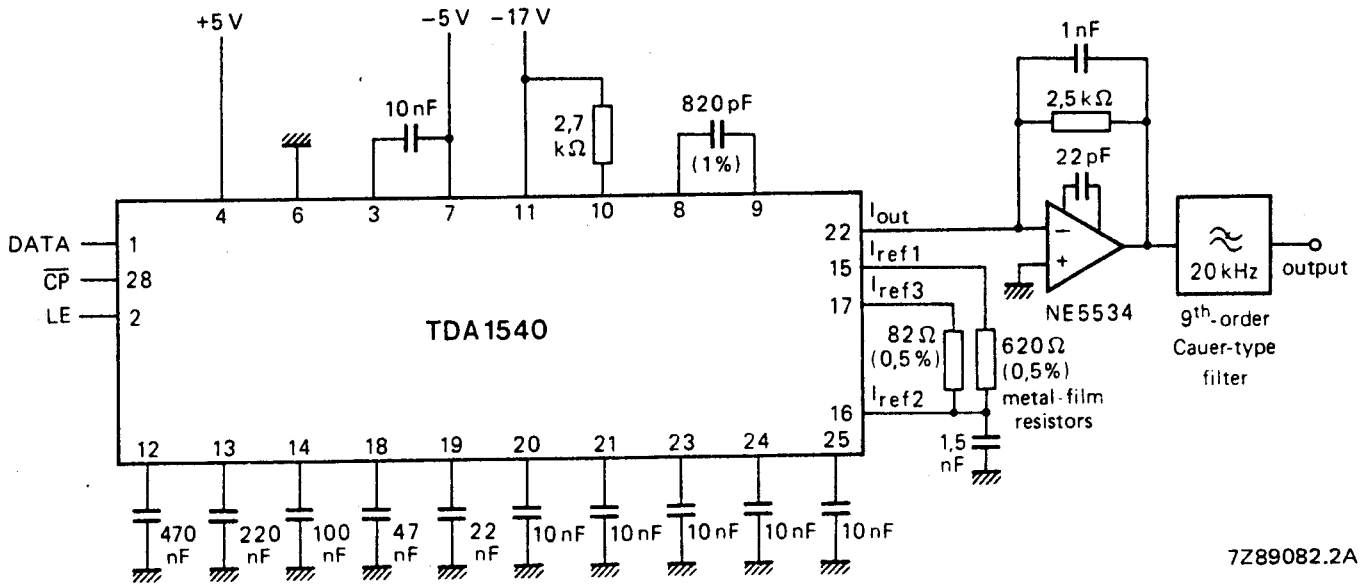
## CHARACTERISTICS (see application circuit Fig. 4)

$T_{amb} = 25\text{ °C}$ ; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>Supply voltages</b>					
with respect to GND (pin 6)					
at pin 4	$V_{P1}$	3	5	7	V
at pin 7	$V_{N1}$	-4,7	-5	-7	V
at pin 11	$V_{N2}$	-16,5	-17	-18	V
<b>Supply currents</b>					
at pin 4*	$I_{P1}$	-	12	14	mA
at pin 7	$I_{N1}$	-	-20	-24	mA
at pin 11	$I_{N2}$	-	-11	-13	mA
<b>Power dissipation</b>					
Total power dissipation	$P_{tot}$	-	350	410	mW
<b>Temperature</b>					
Operating ambient temperature range	$T_{amb}$	-20	-	+70	°C

\* When the output current is  $\frac{1}{2}I_{FS}$  ( $\frac{1}{2}$  full scale output current).

parameter	symbol	min.	typ.	max.	unit
<b>Data input DATA (pin 1)</b>					
Input voltage HIGH	$V_{IH}$	2,0	—	7,0	V
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input current HIGH at $V_{IH}$	$I_{IH}$	—	—	50	$\mu$ A
Input current LOW at $V_{IL}$	$-I_{IL}$	—	—	0,2	mA
Maximum input bit rate	$BR_{max}$	12	—	—	Mbits/s
<b>Latch enable input LE (pin 2)</b>					
<b>Clock input <math>\overline{CP}</math> (pin 28)</b>					
Input voltage HIGH	$V_{IH}$	2,0	—	7,0	V
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input current HIGH at $V_{IH}$	$I_{IH}$	—	—	50	$\mu$ A
Input current LOW at $V_{IL}$	$-I_{IL}$	—	—	0,2	mA
Maximum clock frequency	$f_{CPmax}$	12	—	—	MHz
<b>Oscillator (pins 8 and 9)</b>					
Oscillator frequency at $C_{8,9} = 820$ pF	$f_{osc}$	100	160	200	kHz
<b>Analogue output <math>I_{out}</math> (pin 22)</b>					
Output voltage compliance	$V_{OC}$	-10	—	+ 10	mV
Full scale current	$I_{FS}$	3,8	4,0	4,2	mA
Zero scale current	$\pm I_{ZS}$	—	—	100	nA
Full scale temperature coefficient $T_{amb} = -20$ to $+70$ °C	$TC_{FS}$	—	$\pm 30 \times 10^{-6}$	—	$K^{-1}$
Settling time to $\pm \frac{1}{2}$ LSB all bits on or off	$t_{cs}$	—	0,5	—	$\mu$ s
Signal-to-noise ratio*	S/N	80	85	—	dB



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Fig. 4 Application circuit.

### PINNING

1	DATA	data input
2	LE	latch enable input
3	V <sub>ref1</sub>	voltage reference
4	V <sub>p1</sub>	positive supply
5	i.c.*	frequency compensation on-chip operational amplifier
6	GND	ground
7	V <sub>N1</sub>	negative supply
8	OSC1	} oscillator capacitor
9	OSC2	
10	V <sub>ref2</sub>	voltage reference
11	V <sub>N2</sub>	negative supply
12	C1	} decoupling binary weighted current sources
13	C2	
14	C3	
15	I <sub>ref1</sub>	} current reference sources
16	I <sub>ref2</sub>	
17	I <sub>ref3</sub>	
18	C4	} decoupling binary weighted current sources
19	C5	
20	C6	
21	C7	
22	I <sub>out</sub>	analogue output
23	C8	} decoupling binary weighted current sources
24	C9	
25	C10	
26	i.c.*	voltage reference
27	i.c.*	voltage reference
28	CP	clock pulse input

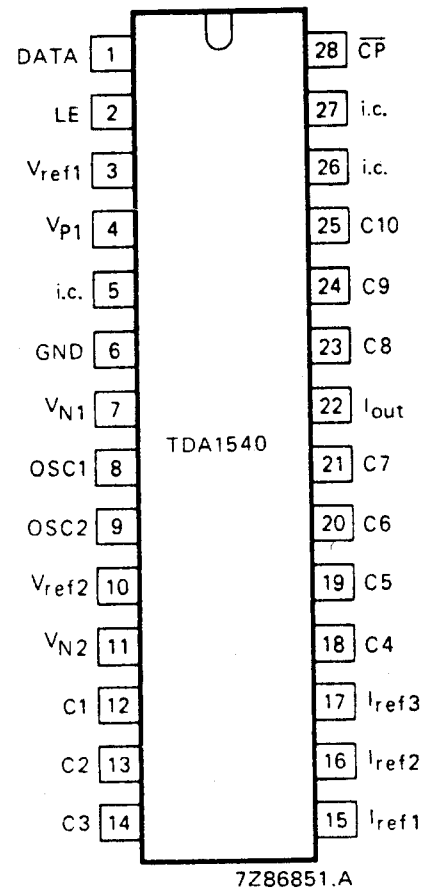


Fig. 5 Pinning diagram.

\* i.c.: internally connected.