Signetics

TDA1540TD, PN
14-Bit DAC (Serial Output)

Product Specification

033018

Linear Products

DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital-to-analog converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85dB in the audio band.

FEATURES

- **Clock frequency 12MHz**
- **Signal-to-noise ratio 85dB**
- **TTL compatible input**
- **On-chip current reference**
- **Inherent monotonicity from −25°C to 70°C**
- **Serial data input**

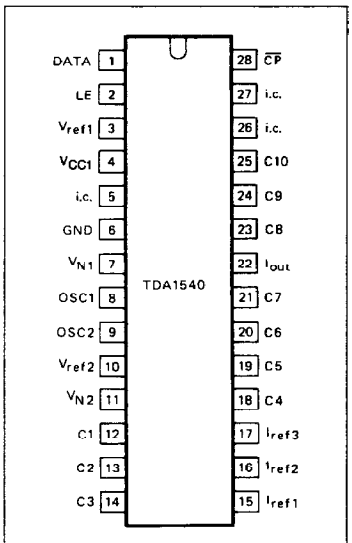
APPLICATIONS

- **Sound reproduction**
- **Recording systems**
- **Graphic display systems**
- **Electron-beam recording**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117BE)	0 to + 70°C	TDA1540PN
28-Pin Plastic SO (SOT-117BE)	0 to + 70°C	TDA1540D

PIN CONFIGURATION



CD10661S

PIN NO.	SYMBOL	DESCRIPTION
1	DATA	Data input
2	LE	Latch enable input
3	V_{REF1}	Voltage reference
4	V_{CC1}	Positive supply
5	IC*	Frequency compensation on-chip operational amplifier
6	GND	Ground
7	V_{N1}	Negative supply
8	OSC1	Oscillator capacitor
9	OSC2	
10	V_{REF2}	Voltage reference
11	V_{N2}	Negative supply
12	C1	Doubling binary
13	C2	Weighted current
14	C3	Sources
15	I_{REF1}	
16	I_{REF2}	Current reference sources
17	I_{REF3}	
18	C4	
19	C5	Decoupling binary weighted
20	C6	Current sources
21	C7	
22	I_{OUT}	Analogue output
23	C8	Decoupling binary
24	C9	Weighted current
25	C10	Sources
26	IC*	Voltage reference
27	IC*	Voltage reference
28	$\overline{CP}$	Clock pulse input

14-Bit DAC (Serial Output) — TDA1540TD, PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
	Supply voltages with respect to GND (Pin 6)		
V_{CC1}	at Pin 4	MAX. 12	V
V_{N1}	at Pin 7	MAX. −12	V
V_{N2}	at Pin 11	MAX. −20	V
$V_{P1} - V_{N2}$	at Pin 4 with respect to Pin 11	MAX. 32	V
$V_{N1} - V_{N2}$	at Pin 7 with respect to Pin 11	−1 to +20	V
P_{TOT}	Total power dissipation	Max. 600	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +80	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ at typical supply voltages unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply voltages with respect to GND (Pin 6)					
V_{CC1}	at Pin 4	3	5	7	V
V_{N1}	at Pin 7	−4.7	−5	−7	V
V_{N2}	at Pin 11	−16.5	−17	−18	V
Supply currents					
I_{CC1}	at Pin 4[1]		12	14	mA
I_{N1}	at Pin 7		−20	−24	mA
I_{N2}	at Pin 11		−11	−13	mA
Power dissipation					
P_{TOT}	Total power dissipation		350	410	mW
Temperature					
T_A	Operating ambient temperature range	−20		+70	°C
Data input DATA (Pin 1)					
V_{IH}	Input voltage HIGH	2.0		7.0	V
V_{IL}	Input voltage LOW	0		0.8	V
I_{IH}	Input current HIGH at V_{IH}			50	μA
$-I_{IL}$	Input current LOW at V_{IL}			0.2	mA
BR_{MAX}	Maximum input bit rate	12			Mbits/s
Latch enable input LE (Pin 2) Clock input $\overline{CP}$ (Pin 28)					
V_{IH}	Input voltage HIGH	2.0		7.0	V
V_{IL}	Input voltage LOW	0		0.8	V
I_{IH}	Input current HIGH at V_{IH}			50	μA
$-I_{IL}$	Input current LOW at V_{IL}			0.2	mA
f_{CPMAX}	Maximum clock frequency	12			MHz
Oscillator (Pins 8 and 9)					
f_{OSC}	Oscillator frequency at $C_{8-9} = 820pF$	100	160	200	kHz

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ at typical supply voltages unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Analog output I_{OUT} (Pin 22)					
V_{OC}	Output voltage compliance	-10		+10	mV
I_{FS}	Full-scale current	3.8	4.0	4.2	mA
$\pm I_{ZS}$	Zero-scale current			100	nA
TC_{FS}	Full-scale temperature coefficient $T_A = -20$ to $+70°C$		$\pm 30 \times 10^{-6}$		$°C^{-1}$
t_{CS}	Settling time to $\pm \frac{1}{2}$ LSB all bits on or off		0.5		μs
S/N	Signal-to-noise ratio[2]	80	85		dB

NOTES:
1. When the output current is $\frac{1}{2}I_{FS}$ ($\frac{1}{2}$ full-scale output current).
2. Signal-to-noise ratio within 20Hz and 20kHz full-scale sinewave, generated at a sample rate of 44kHz.

FUNCTIONAL DESCRIPTION

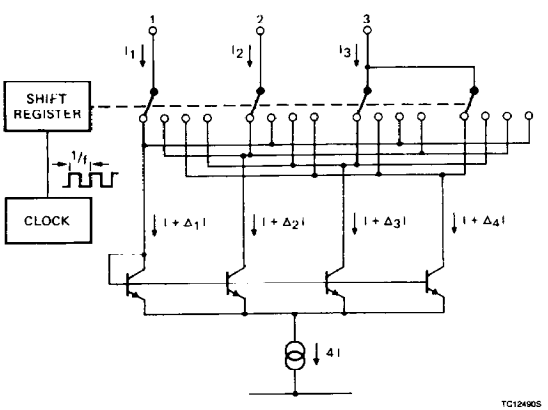
The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an AC low-pass filter, requiring an external filter capacitor.

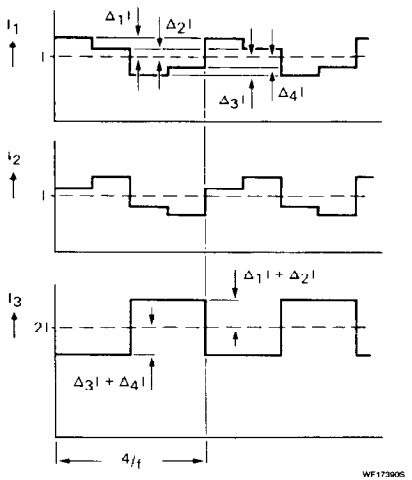
The outputs of the dividers are combined to obtain the output currents I (I_1), I(I_2) and 2I (I_3) (see Figure 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Figure 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (Pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0V ± 10mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Figure 4.



a. Circuit Diagram of One Divider Stage



b. Waveforms Showing Output Currents I_1, I_2 and I_3 of Figure 1a

Figure 1

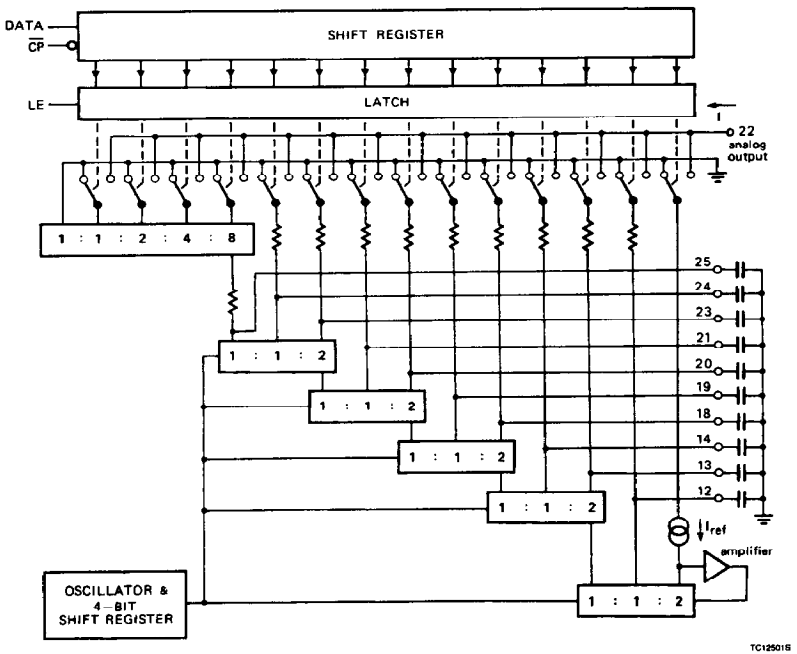


Figure 2. Functional Diagram Showing Cascading of Current Division Stages

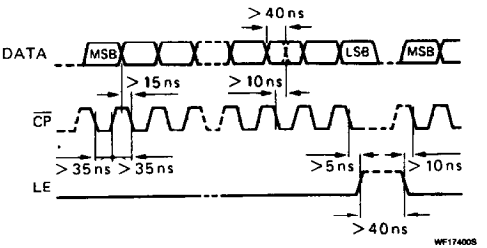


Figure 3. Format of Input Signals

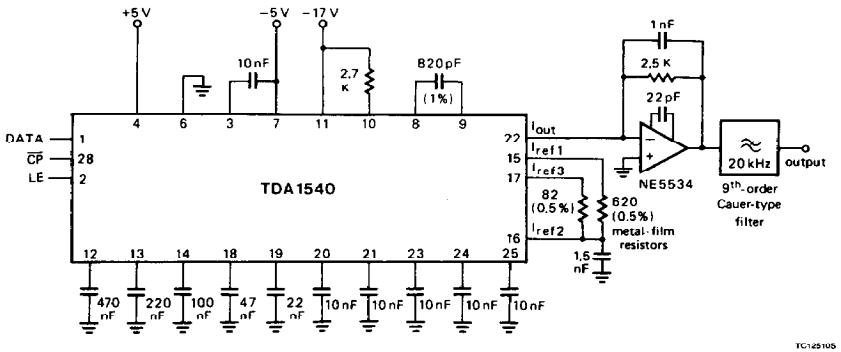


Figure 4. Application Circuit