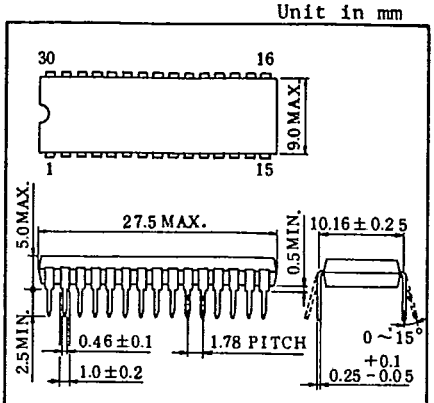
TD6720N

16-BITS Hi-Fi D/A CONVERTER

TD6720N is a dual-slope single-integral system 16-bits Hi-Fi D/A converter designed for use in PCM digital audio equipments.

- Corresponding with sampling frequency from 30kHz to 100kHz.
  (Suitable for two times over sampling D/A system in CD player and DAT.)
- X'tal oscillation amp. is built in.
- X'tal 1/4-divided clock is output from SCK terminal.
- Both signals of right and left stereo channels are alternatively D/A-converted.
- Sample-hold circuit is built in to reduce external parts.
- Corresponding with 2's complement code.
- S/N : 90dB TYP.
  THD : 0.003% TYP.

Unit in mm



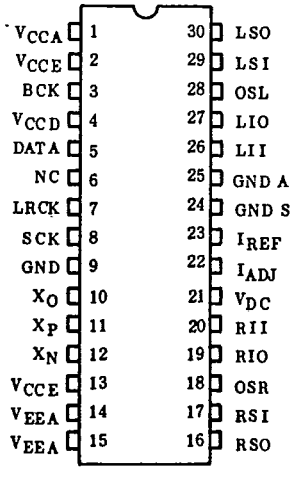
Lead pitch is 1.78 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.30 leads.

JEDEC	—
TOSHIBA	4D30A-P

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage (+)	V_{CC}	0~5.5	V
Power Supply Voltage (-)	V_{EE}	0~-5.5	V
Power Dissipation	P_D	1500	mW
Operating Temperature	Topr	-25~75	°C
Storage Temperature	Tstg	-55~150	°C

PIN CONNECTIONS



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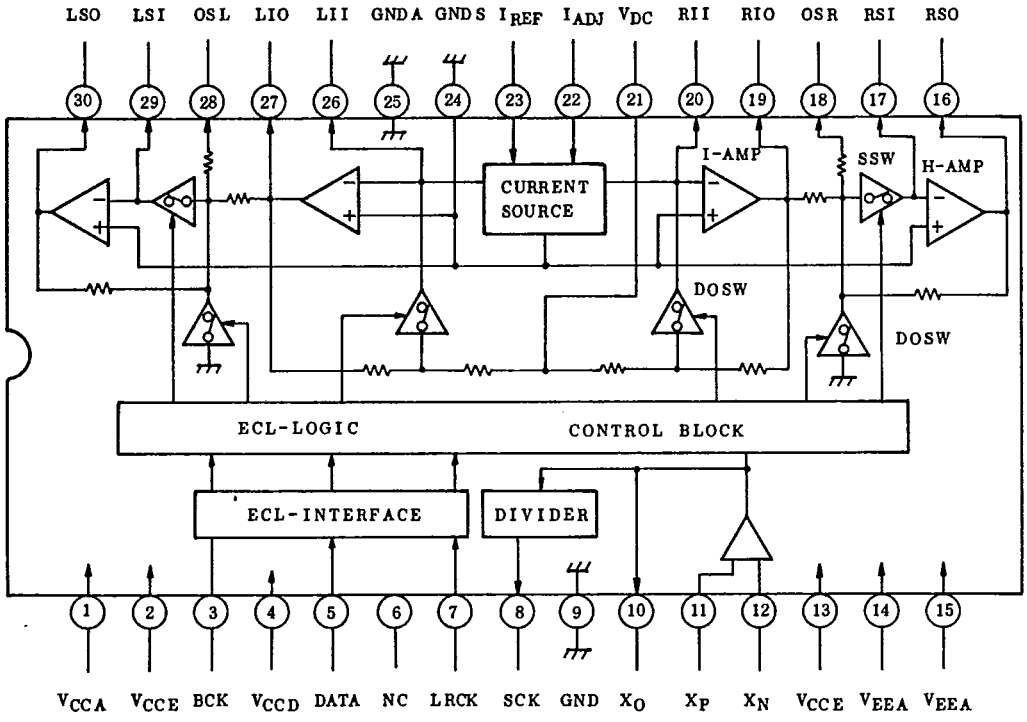
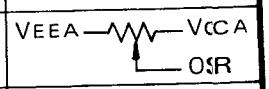
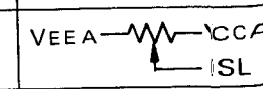
BLOCK DIAGRAM



Terminal Function Description

Pin No.	Name	Function and Operation	Note
1	VCCA	Analog plus power supply voltage terminal. +5V	
2	VCCE	ECL logic power supply voltage terminal. +5V	
3	BCK	Bit clock input terminal. Duty cycle = 50%, f = 1.4112 MHz	
4	VCCD	Digital power supply voltage terminal. +5V	
5	DATA	PCM digital audio data input terminal. Inputs in bit serial (16 bit) from MSB synchronized with BCK falling edge.	
6	NC	Not connected.	
7	LRCK	Input data, Lch and Rch indication signal input terminal. Inputs synchronized with BCK falling edge.	
8	SCK	Divided clock signal output.	
9	GND	Ground terminal.	
10 11 12	XO XP XN	Oscillator input/output terminal. Constitutes deformed Colpitts oscillator circuit by combining L, C & R with SAW resonator or X'tal oscillator.	
13	VCCE	ECL logic power supply voltage terminal. +5V	
14, 15	VEEA	Analog minus power supply voltage terminal. −5V	
16	RSO	Rch sample and hold amp output terminal.	
17	RSI	Rch sample and hold and minus input terminal.	
18	OSR	Rch output offset adjustment terminal. Normally connected to GND A.	
19	RIO	Rch integral amp output terminal.	
20	RII	Rch integral amp minus input terminal.	
21	VDC	Discharge circuit reference voltage terminal.	
22	IADJ	Current source fine adjustment terminal. Normally connected to GND A.	
23	IREF	Reference current input terminal.	
24	GND S	Ground terminal.	
25	GND A	Analog ground terminal.	
26	LII	Lch integral amp minus input terminal.	
27	LIO	Lch integral amp output terminal.	
28	OSL	Lch output offset adjustment terminal. Normally connected to GND A.	
29	LSI	Lch sample and hold amp minus input terminal.	
30	LSO	Lch smaple and hold amp output terminal.	