NIPPON PRECISION CIRCUITS LTD.

CMOS LSI ΣDECO SM5864AP

Digital Audio D/A Converter

OVERVIEW

The ΣDECO SM5864AP D/A converter is a high-speed converter for digital audio systems fabricated using NPC's molybdenum-gate CMOS process. A selectable operating frequency and balanced outputs allow the ΣDECO SM5864AP to be adapted to a wide range of applications.

The ΣDECO SM5864AP is designed to be used with a digital eight-times oversampling filter and has two serial inputs for left- and right-channel data. The serial input data format consists of 20-bit words in 2s complement, with the most significant bit first.

The ΣDECO SM5864AP linearly interpolates the input signal at a high multiple of the original sampling frequency and then requantizes the resulting signal. A fourth-order noise shaper is used to remove most of the quantizing noise before the signal is output as a pulsewidth-modulated (PWM) waveform. Quasi-symmetrical PWM outputs allow the use of low system clock frequencies.

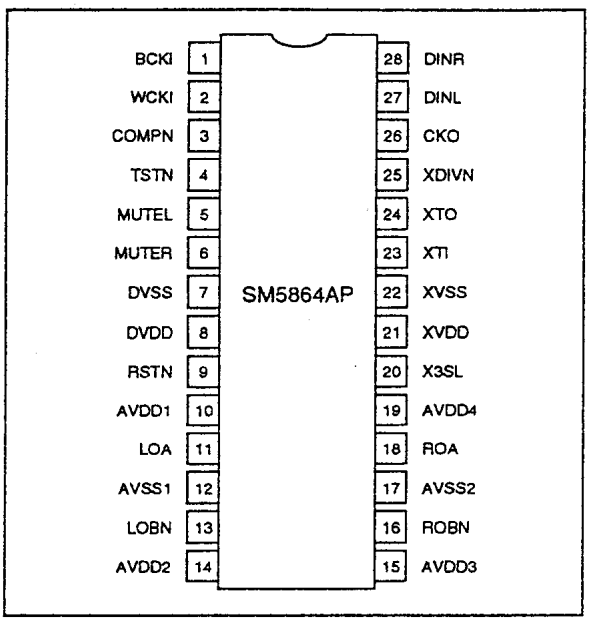
The ΣDECO SM5864AP has a complementary output mode that produces a single low-distortion, high-linearity output channel.

The ΣDECO SM5864AP operates from a single 5 V supply and is available in 28-pin plastic DIPs.

FEATURES

- Two-channel D/A converter
- Designed for use with a digital eight-times oversampling filter.
- Quasi-symmetrical PWM outputs
- High-accuracy pulsewidth-modulated output
- 384fs, 768fs, 512fs or 1024fs selectable system clock frequencies
- On-chip crystal oscillator circuit
- Fourth-order, 32fs noise shaper
- TTL-compatible inputs and outputs
- Molybdenum-gate CMOS process
- Single 5 V supply
- 28-pin plastic DIPs

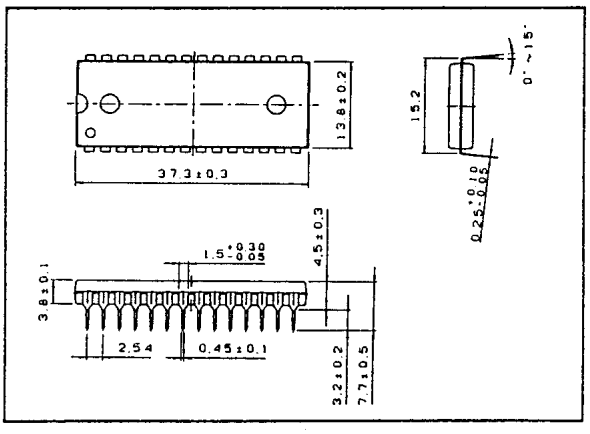
PINOUT



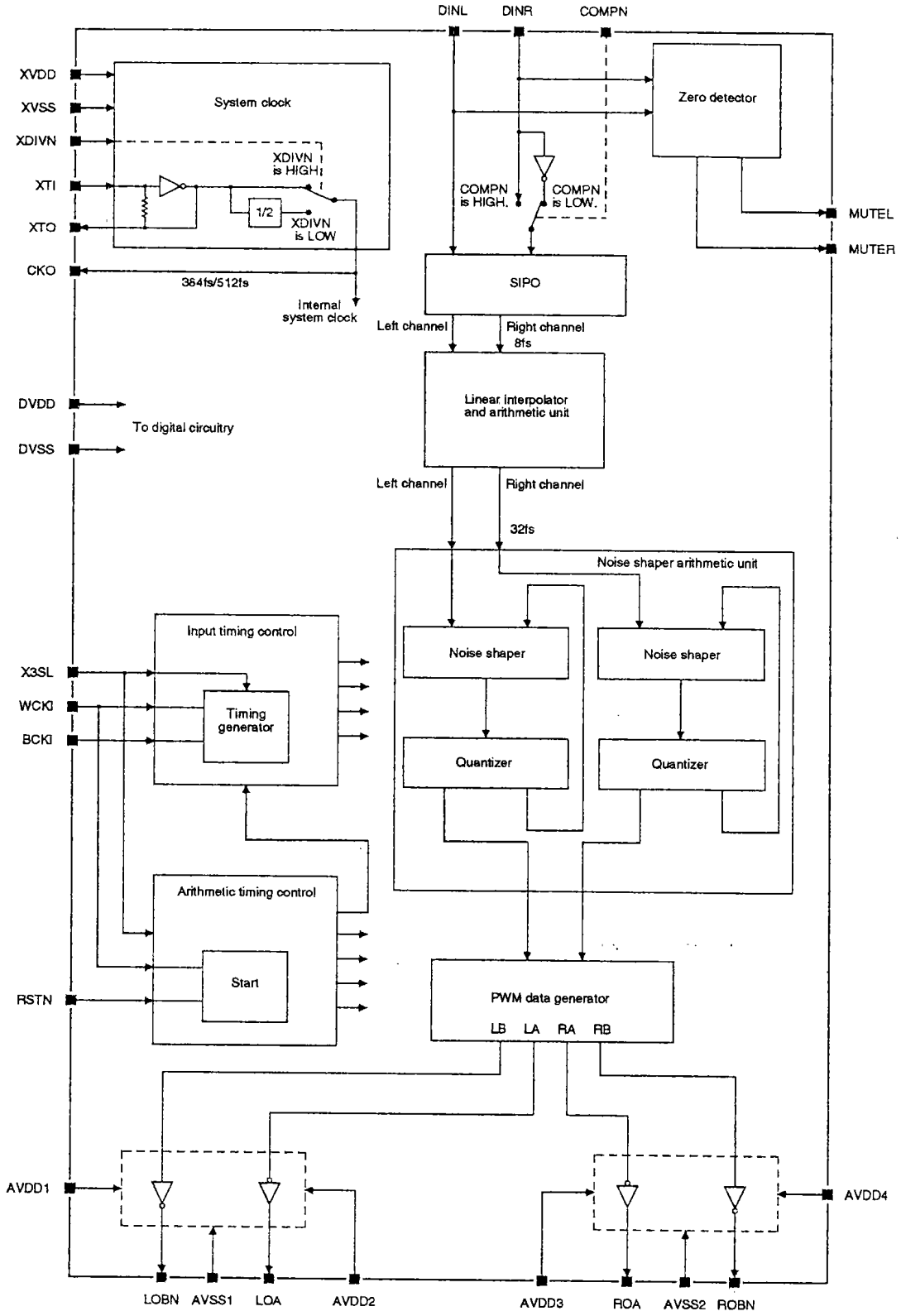
PACKAGE DIMENSIONS

Unit: mm

Plastic DIP28



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	BCKI	Bit clock input. Data is latched into the input shift registers on the rising edge of BCKI. Internal pull-up resistor
2	WCKI	Word clock input. Words are latched into the converter input registers on the falling edge of WCKI. Internal pull-up resistor
3	COMPN	PWM output mode select input. Internal pull-up resistor
4	TSTN	Test input. Tie HIGH or leave open. Internal pull-up resistor
5	MUTEL	Left-channel mute control output
6	MUTER	Right-channel mute control output
7	DVSS	Digital ground
8	DVDD	Digital supply
9	RSTN	Reset input. Active-LOW. Internal pull-up resistor
10	AVDD1	Analog supply 1
11	LOA	Left-channel positive PWM output
12	AVSS1	Analog ground 1
13	LOBN	Left-channel negative PWM output
14	AVDD2	Analog supply 2
15	AVDD3	Analog supply 3
16	ROBN	Right-channel negative PWM output
17	AVSS2	Analog ground 2
18	ROA	Right-channel positive PWM output
19	AVDD4	Analog supply 4
20	X3SL	Clock frequency select input. Internal pull-up resistor
21	XVDD	Clock supply
22	XVSS	Clock ground
23	XTI	Crystal oscillator or external clock input
24	XTO	Crystal oscillator output
25	XDIVN	System clock frequency select input. Internal pull-up resistor
26	CKO	384fs or 512fs clock output
27	DINL	Left-channel serial data input. Internal pull-up resistor
28	DINR	Right-channel serial data input. Internal pull-up resistor

Note

fs is the sampling rate. fs is normally 44.1 kHz for CD data.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	–0.3 to 7.0	V
Input voltage range for all inputs except XTI	V_{IN1}	DV_{SS} – 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{IN2}	XV_{SS} – 0.3 to XV_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opr}	–20 to 80	deg. C
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{SLD}	255	deg. C
Soldering time	t_{SLD}	10	s

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	DV_{DD}, AV_{DD}, XV_{DD}	5	V
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	4.75 to 5.25	V
Supply voltage differential	DV_{DD} – XV_{DD}, DV_{DD} – AV_{DD}, XV_{DD} – AV_{DD}, DV_{SS} – XV_{SS}, DV_{SS} – AV_{SS}, XV_{SS} – AV_{SS}	–0.1 to 0.1	V

Note

All power supply pins (VDD and VSS) should be connected to the same external power supply.

DC Electrical Characteristics

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 4.75 to 5.25 V, T_a = –20 to 80 deg. C unless otherwise specified

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 5 V, f_{XTI} = 49.2 MHz, no load. XDIVN is LOW. X3SL is LOW.	–	22	35	mA
Analog circuitry supply current	I_{DDA}		–	2.5	5	mA
Clock circuitry supply current	I_{DDX}		–	8	15	mA
LOW-level input voltage	V_{IL2}	See note 1.	–	–	0.5	V
HIGH-level input voltage	V_{IH2}		2.4	–	–	V
XTI LOW-level input voltage	V_{IL1}	External clock input	–	–	0.3XV_{DD}	V
XTI HIGH-level input voltage	V_{IH1}		0.7XV_{DD}	–	–	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3XV_{DD}	–	–	V_{p-p}
PWM LOW-level output voltage	V_{OLA}	I_{OL} = 2 mA. See note 3.	–	–	0.3	V
PWM HIGH-level output voltage	V_{OHA}	I_{OH} = –2 mA. See note 3.	AV_{DD} – 0.3	–	–	V
LOW-level output voltage	V_{OL1}	I_{OL} = 1.6 mA. See note 2.	–	–	0.4	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH1}	I_{OH} = –0.4 mA. See note 2.	2.5	–	–	V
CKO LOW-level output voltage	V_{OL2}	I_{OL} = 1.6 mA	–	–	0.5	V
CKO HIGH-level output voltage	V_{OH2}	I_{OH} = –0.4 mA	2.5	–	–	V
LOW-level input current	I_{IL2}	V_{IN} = 0 V. See note 1.	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	10	20	µA
XTI HIGH-level input current	I_{IH1}	V_{IN} = XV_{DD}	–	10	20	µA
Input leakage current	I_{LH}	V_{IN} = DV_{DD}. See note 1.	–	–	1	µA

Notes

1. DINL, DINR, BCKI, WCKI, COMPN, TSTN, RSTN, XDIVN, X3SL
2. MUTEL, MUTER
3. LOA, LOBN, ROA, ROBN

AC Electrical Characteristics

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, DV_{DD} = AV_{DD} = XV_{DD} = 4.75 to 5.25 V, T_a = –20 to 80 deg. C unless otherwise specified

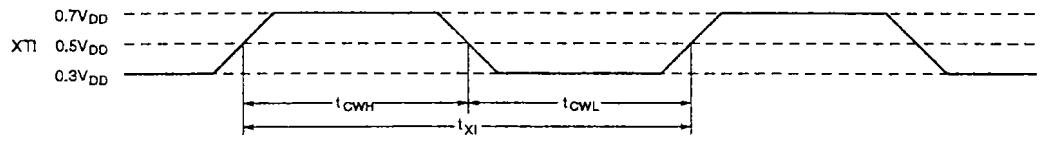
System clock

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Clock frequency	fosc	Crystal oscillator connected to XTI and XTO	X3SL and XDIVN are HIGH.	2.0	16.9	20.0	MHz
			X3SL is HIGH. XDIVN is LOW.	4.0	33.9	39.5	
			X3SL is LOW. XDIVN is HIGH.	4.0	24.6	27.5	
			X3SL and XDIVN are LOW.	8.0	49.2	51.5	
External clock LOW-level pulsewidth	t_{CWL}	X3SL and XDIVN are HIGH.		23.0	29.5	250.0	ns
		X3SL is HIGH. XDIVN is LOW.		12.0	14.7	125.0	
		X3SL is LOW. XDIVN is HIGH.		16.5	20.3	125.0	
		X3SL and XDIVN are LOW.		8.3	10.1	62.0	
External clock HIGH-level pulsewidth	t_{CWH}	X3SL and XDIVN are HIGH.		23.0	29.5	250.0	ns
		X3SL is HIGH. XDIVN is LOW.		12.0	14.7	125.0	
		X3SL is LOW. XDIVN is HIGH.		16.5	20.3	125.0	
		X3SL and XDIVN are LOW.		8.3	10.1	62.0	
External clock period	t_{XI}	X3SL and XDIVN are HIGH.		50.0	59.0	500.0	ns
		X3SL is HIGH. XDIVN is LOW.		25.3	29.5	250.0	
		X3SL is LOW. XDIVN is HIGH.		36.5	40.7	250.0	
		X3SL and XDIVN are LOW.		19.5	20.3	125.0	

Note

Typical ratings are based on 44.1 kHz (X3SL is HIGH) and 48.0 kHz (X3SL is LOW) sampling frequencies.

Clock timing waveform



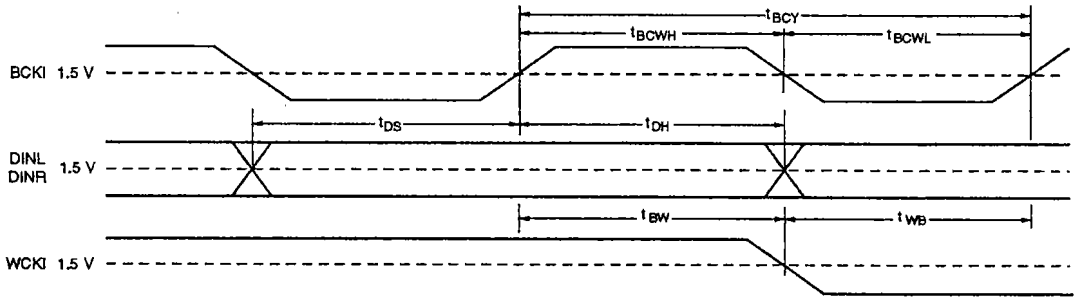
Reset timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reset LOW-level pulsewidth	t_{RSTN}	At power-up	1	–	–	µs
		At times other than power-up	20	–	–	ns

Serial input timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKI LOW-level pulsewidth	t_{BCWL}		30	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH}		30	–	–	ns
BCKI period	t_{BCY}		60	–	–	ns
DINL and DINR setup time	t_{DS}		20	–	–	ns
DINL and DINR hold time	t_{DH}		20	–	–	ns
BCKI to WCKI delay time	t_{BW}		30	–	–	ns
WCKI to BCKI delay time	t_{WB}		20	–	–	ns

Serial input timing waveform



AC Analog Characteristics

DV_{DD} = AV_{DD} = XV_{DD} = 5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, XDIVN and X3SL are HIGH, external crystal oscillator clock input, f_{osc} = 16.9344 MHz, T_a = 25 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion and noise	THD + N	f = 1 kHz, V_I = 0 dB	–	0.0015	0.002	%
Output level	V_{OUT}	f = 1 kHz, V_I = 0 dB	1.8	2.0	2.2	V_{rms}
Dynamic range	D.R	f = 1 kHz, V_I = –60 dB	95	98	–	dB
Signal-to-noise ratio	S/N	f = 1 kHz, V_I = 0 to –∞ dB	100	104	–	dB
Channel separation	Ch. Sep	f = 1 kHz, V_I = –∞ dB	85	95	–	dB

Note

Parameters measured in accordance with EIAJ Standard CP-307.

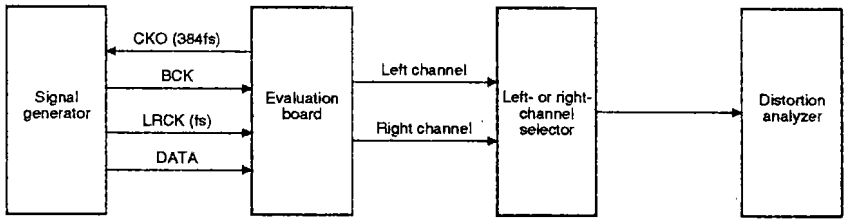
Measurement Circuits

Measurement conditions

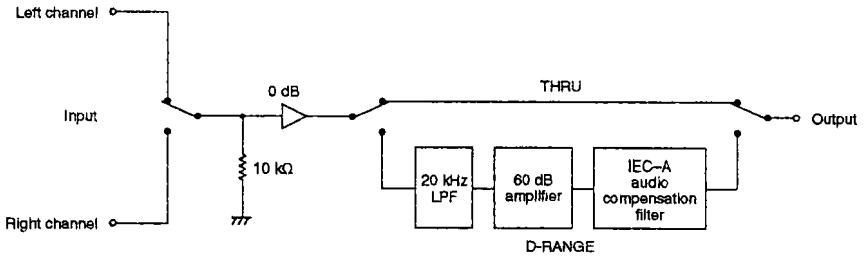
Parameter	Symbol	3346A channel selector position	AD725C distortion analyzer setting
Total harmonic distortion and noise	THD + N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.
Output level	V_{OUT}		
Dynamic range	D.R	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF. JIS* A-weighted filter is ON.
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.

* Japanese Industrial Standard

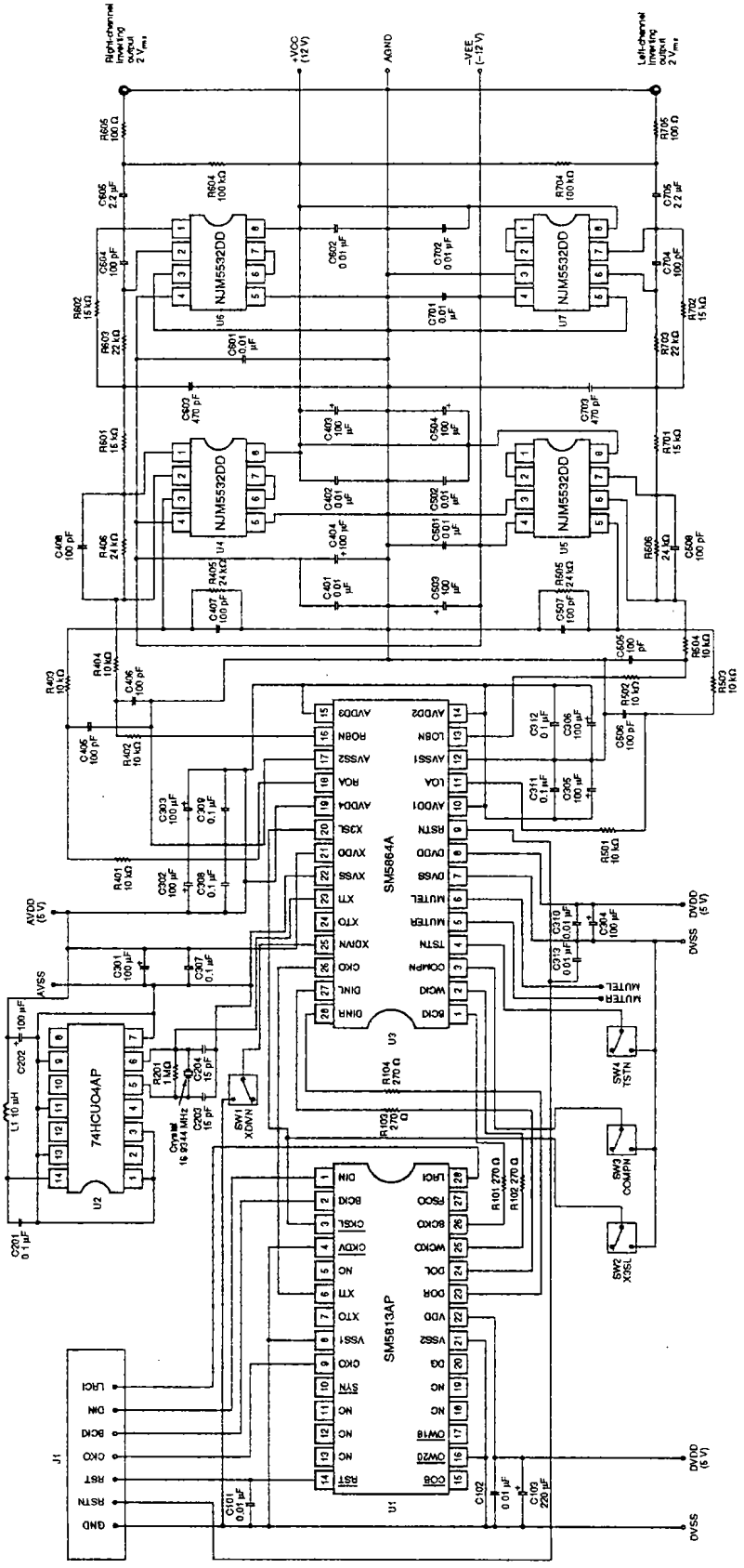
Measurement circuit block diagram



Channel selector internal circuit

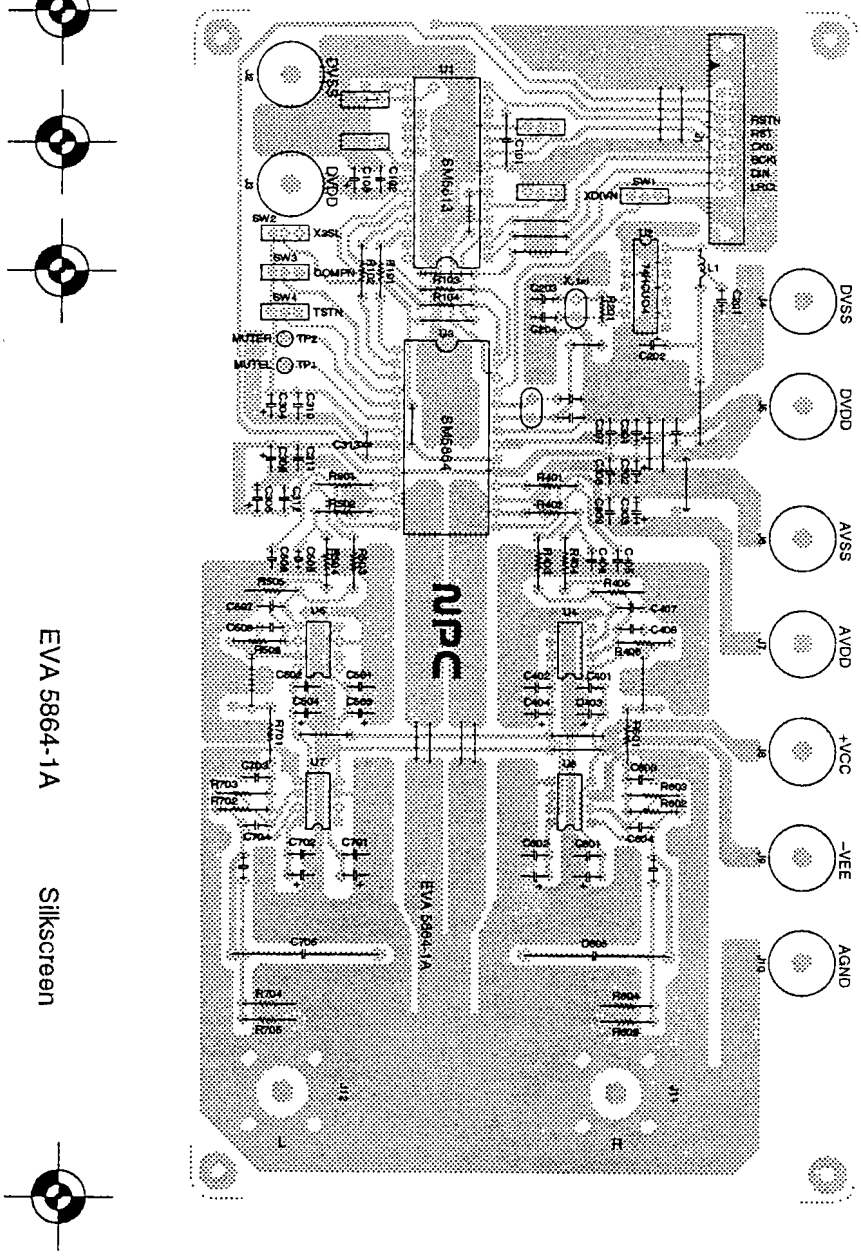


Evaluation board circuit



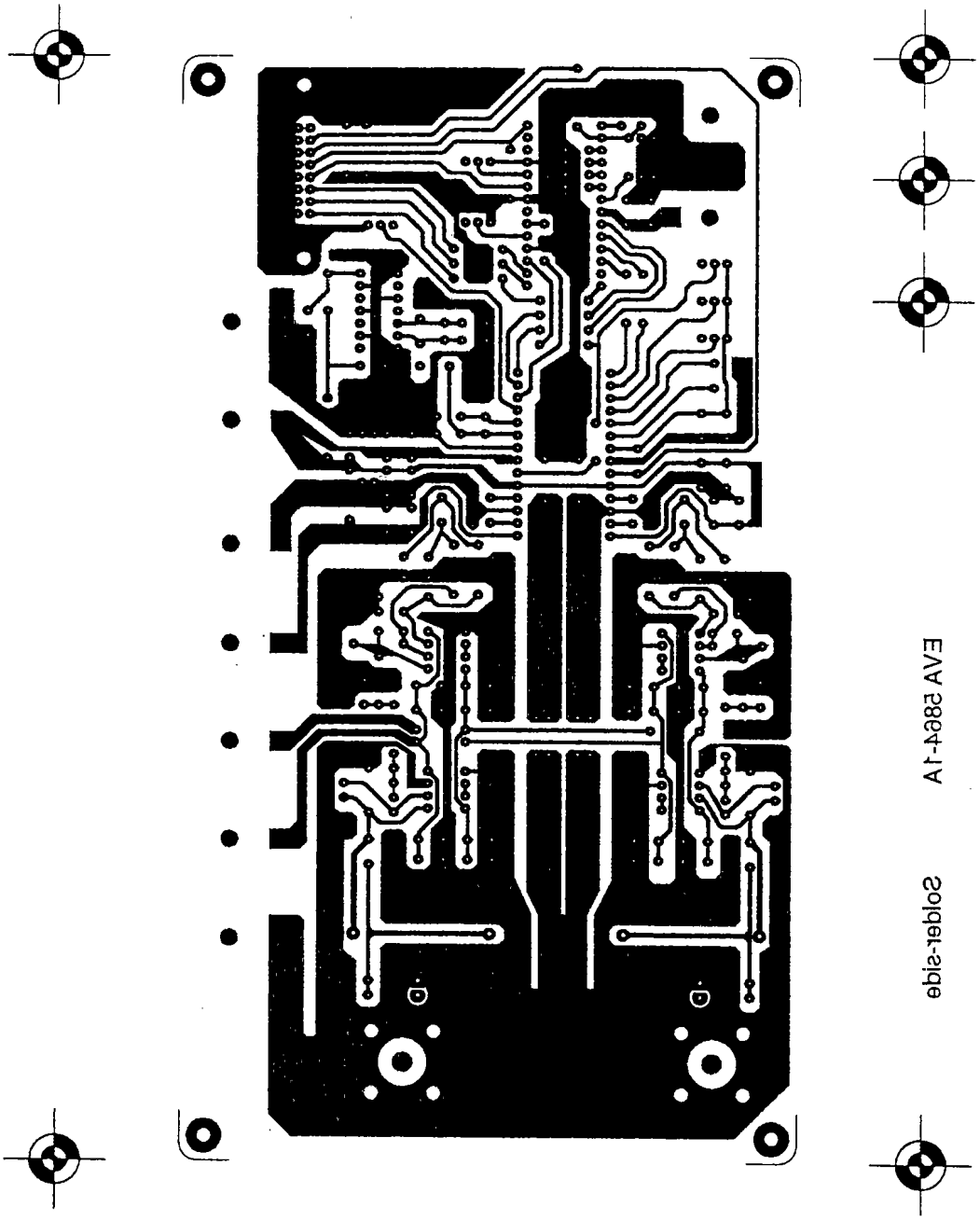
Component layout

The following figure has been reduced by 30%.



PCB pattern

The following figure has been reduced by 30%.



FUNCTIONAL DESCRIPTION

System Clock

XDIVN and X3SL select the system clock frequency as a function of the sampling rate, fs. The effect of XDIVN and X3SL on the system clock and CKO output frequencies is shown in table 1.

Table 1. System clock selection

X3SL	XDIVN	Clock frequency	CKO output frequency
LOW	LOW	1024fs	512fs
LOW	HIGH	512fs	512fs
HIGH	LOW	768fs	384fs
HIGH	HIGH	384fs	384fs

As the stability and signal-to-noise ratio of the system clock greatly affects the AC analog characteristics, care should be taken to ensure that the clock is free from jitter.

The system clock can be controlled by a crystal oscillator, connected as shown in figure 1. Capacitors C1 and C2 should be chosen to match the crystal oscillator used. The system clock can also be supplied externally as shown in figure 2. When using this method, XTO should be left unconnected.

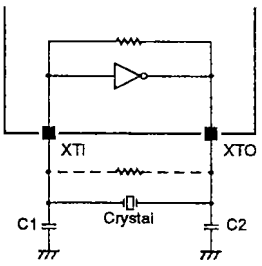


Figure 1. Crystal oscillator connections

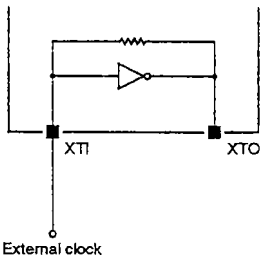


Figure 2. External clock input

Output Modes

The ΣDECO SM5864AP has two output modes, normal and complementary. When COMPN is HIGH, normal mode is selected. The device then converts and outputs both the left and right channels as shown in figure 3.

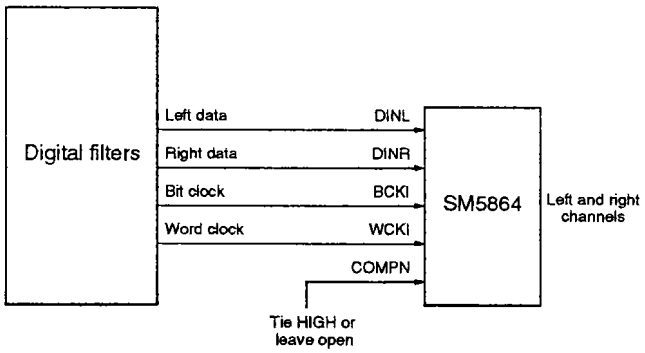


Figure 3. Normal output configuration

When COMPN is LOW, complementary mode is selected and the ΣDECO SM5864AP converts only one channel. Two devices are needed to process both the left and right channels as shown in figure 4. This configuration results in improved distortion and interchannel crosstalk characteristics.

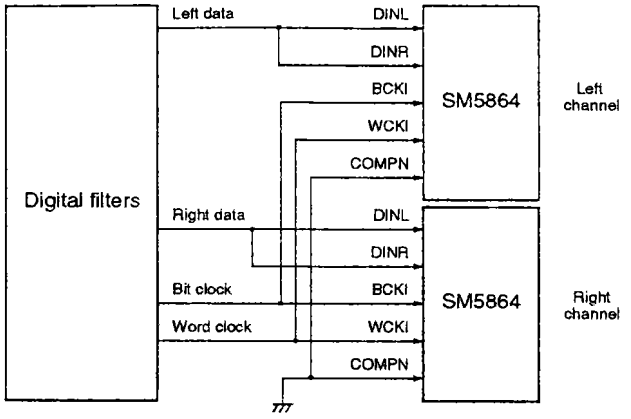


Figure 4. Complementary output configuration

Pulsewidth Modulation Waveforms

The signals output by the ΣDECO SM5864AP are quasi-symmetrical. Each individual output signal is not symmetrical about the center of the output pulses, however the difference signals (LOA – LOBN) and (ROA – ROBN) are symmetrical as shown in figure 5.

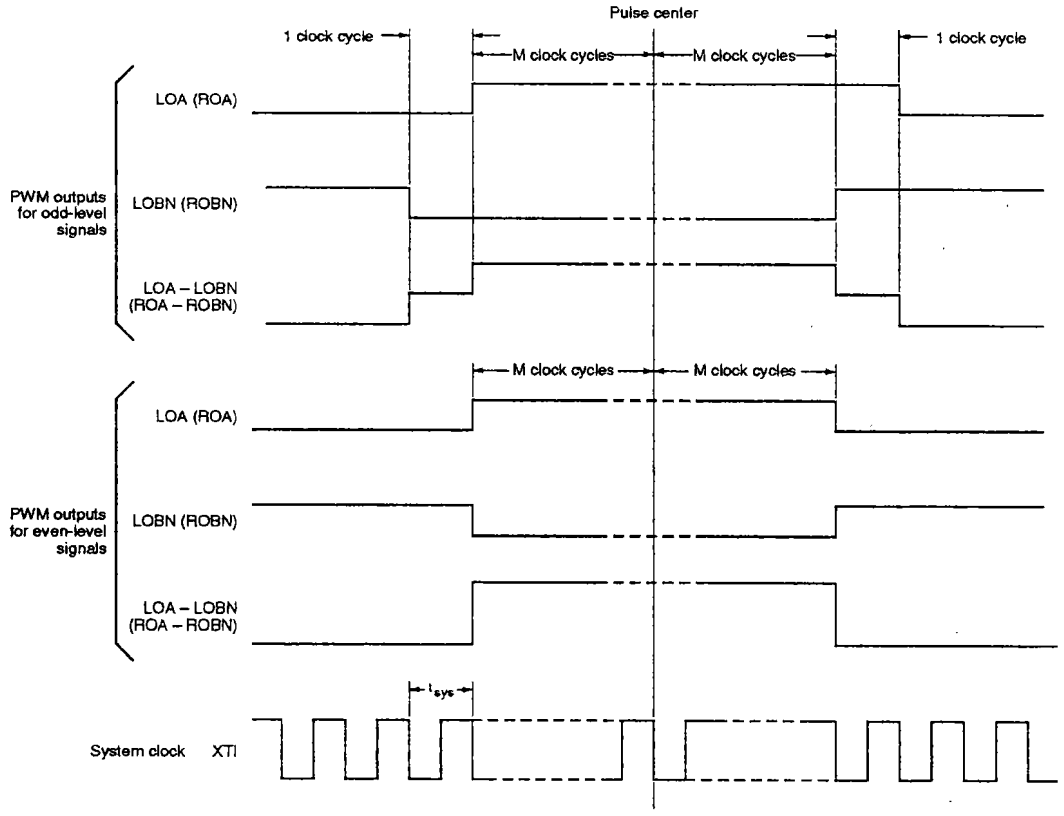


Figure 5. PWM output waveforms

Reset

At power-on, or after a change in system parameters, the input data timing may be corrupted. A LOW-level pulse on RSTN will resynchronize the ΣDECO SM5864AP with the preceding oversampling filter stage.

Upon reset, the following takes place:

1. The internal timing is resynchronized on the falling edge of the 65th cycle of WCKI after RSTN goes HIGH.
2. The PWM outputs are muted with a 50% duty cycle signal from the time when RSTN goes LOW until the rising edge of the 96th cycle of WCKI after RSTN goes HIGH.

Mute Detection

When the serial input data on DINL and DINR remains zero for 2^{21} consecutive bits, the corresponding mute output (MUTEL or MUTER) goes HIGH. Note that the two least significant bits of each word are ignored. If the data remains zero for a further 2^{21} bits, the PWM output changes to a 50% duty cycle waveform, suppressing unnecessary noise. A 50% duty cycle waveform corresponds to the analog ground level after lowpass filtering. For a 44.1 kHz sampling rate and 18-bit word length, 2^{21} bits correspond to a period of approximately 330 ms. Muting operates independently for each channel.

Linear Interpolator

The linear interpolator oversamples the 8fs input signal at the 32fs noise shaper operating frequency. The frequency characteristic of the linear interpolator is shown in figure 6.

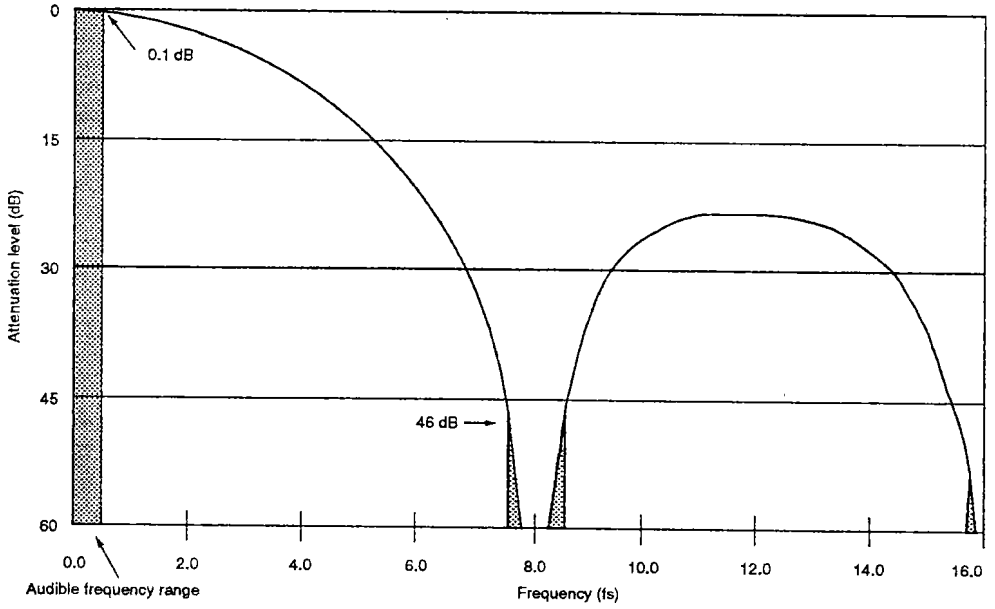


Figure 6. Linear interpolator frequency characteristic

Noise Shaper

A fourth-order noise shaper is implemented on the ΣDECO SM5864AP to eliminate quantization noise in the audio band. The noise shaper uses an NPC proprietary technique which shifts the zero point of the quantization noise processed by the noise shaper. Figure 7 shows the quantization noise component of the signal before the PWM output stage relative to the quantization noise of a non-oversampled 16-bit signal.

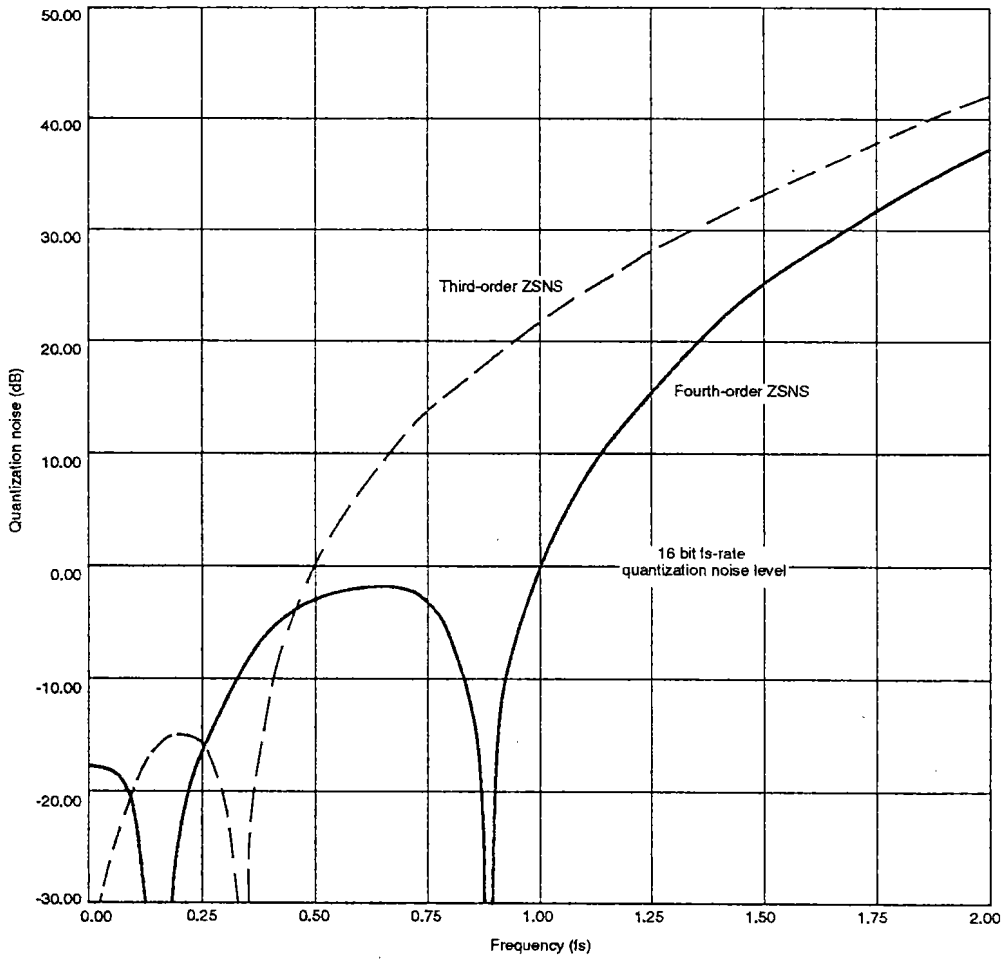


Figure 7. Noise shaper characteristic

DATA FORMAT WAVEFORMS

Audio Data Input

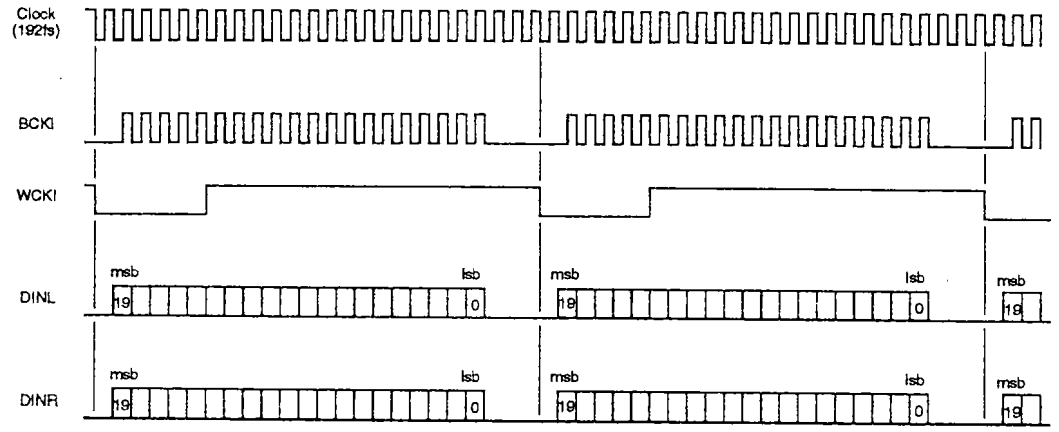


Figure 8. Audio data format 1

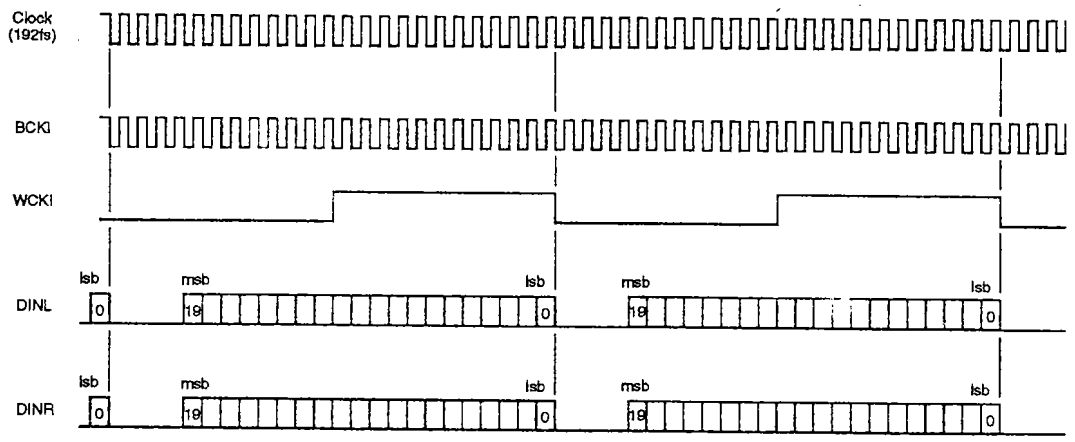


Figure 9. Audio data format 2

APPLICATION NOTES

Input Interfaces

Interface to SM5813 digital eight-times oversampling filter

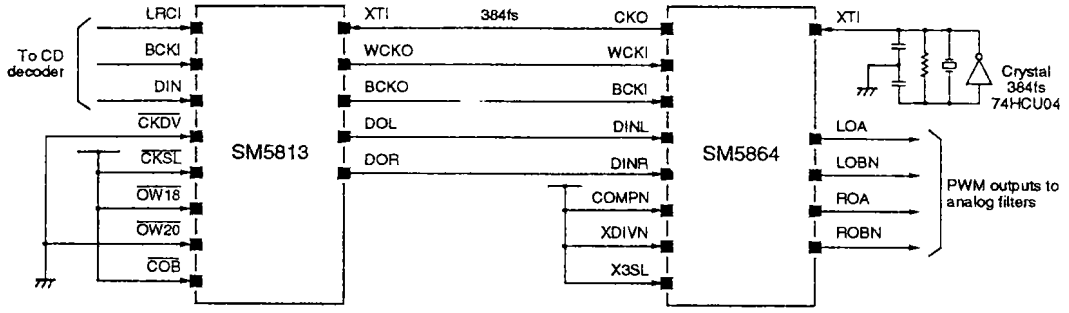


Figure 10. SM5813 interface 1

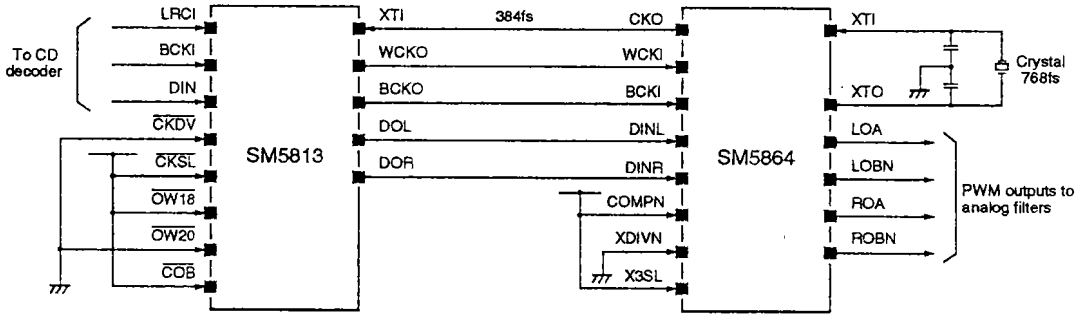


Figure 11. SM5813 interface 2

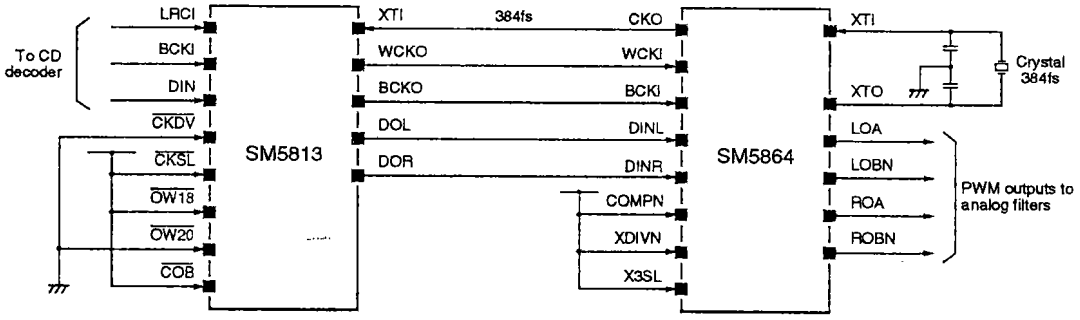


Figure 12. SM5813 interface 3

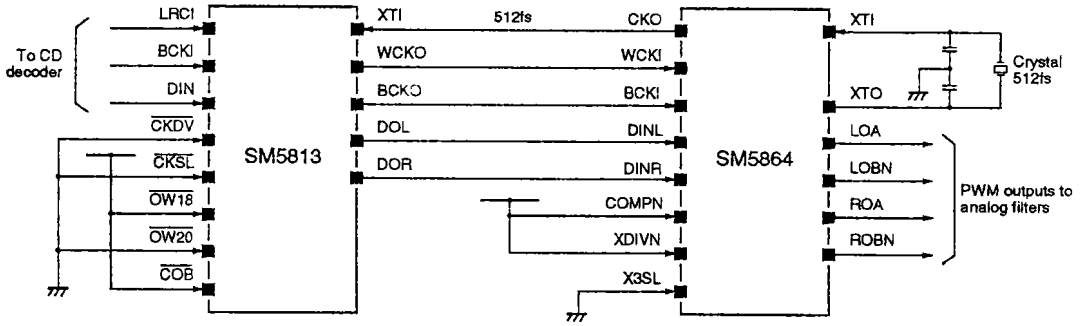


Figure 13. SM5813 interface 4

Interface to SM5840A digital eight-times oversampling filter

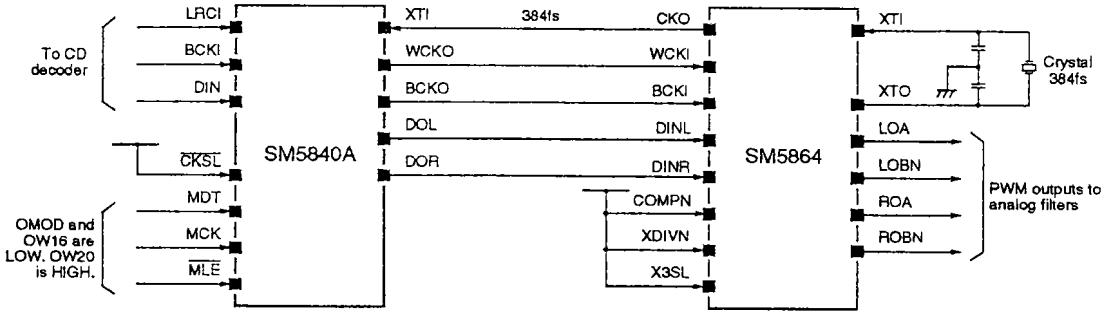


Figure 14. SM5840A interface

Interface to SM5840C digital eight-times oversampling filter

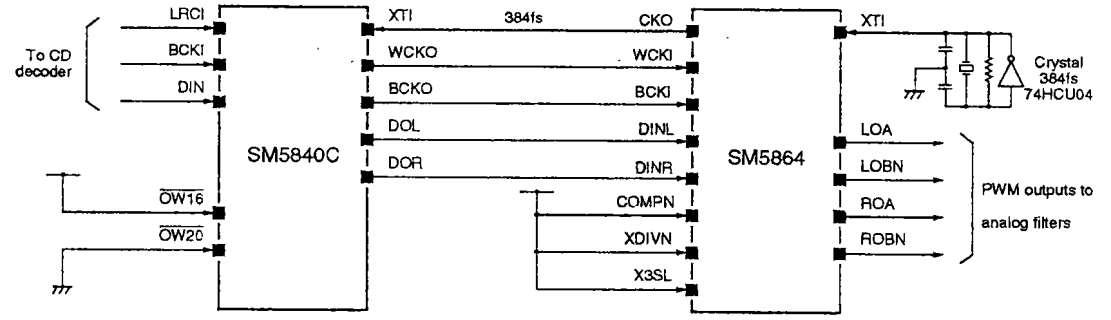


Figure 15. SM5840C interface 1

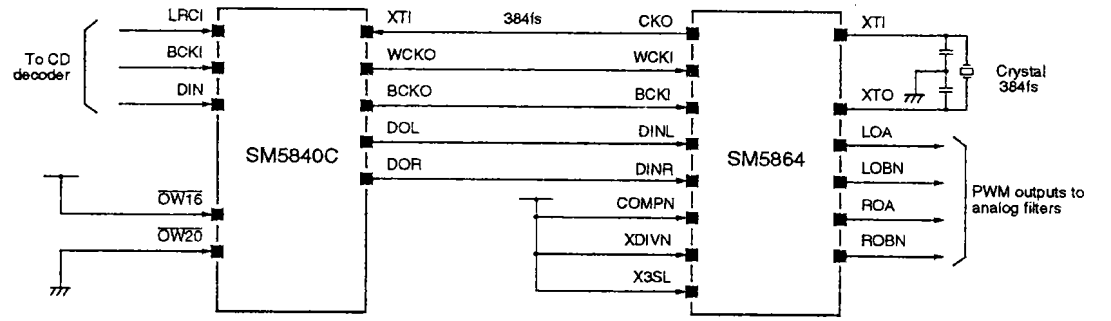


Figure 16. SM5840C interface 2

Output Interfaces

To avoid duplication, only the left channel has been shown in the following figures.

Normal output mode

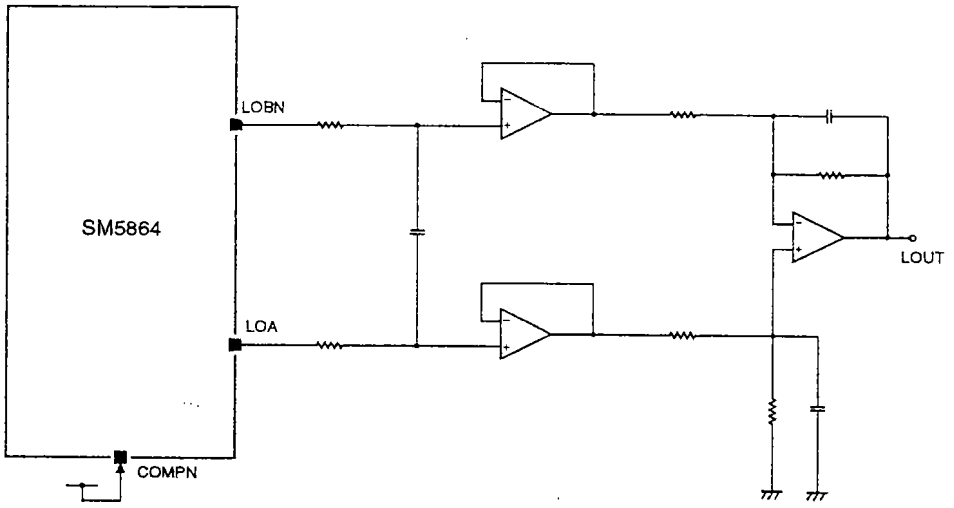


Figure 17. Normal output mode circuit 1

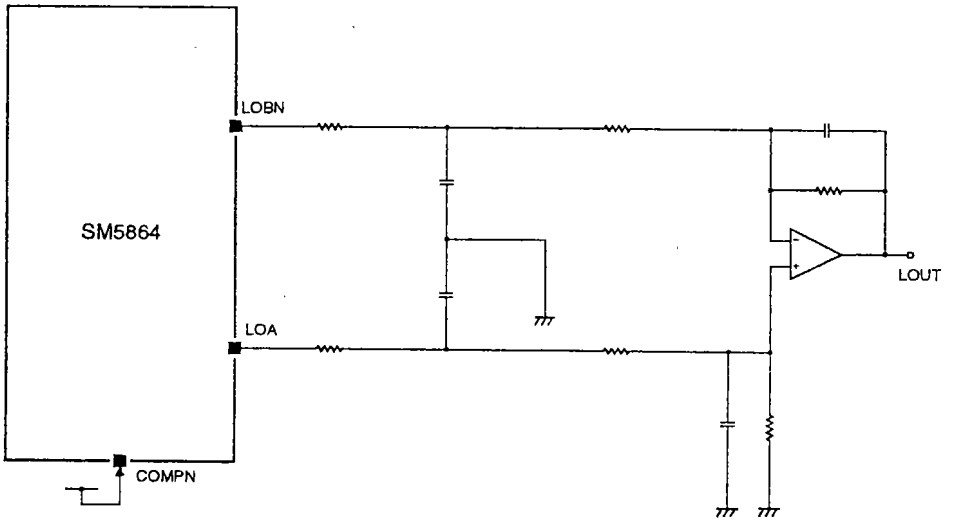


Figure 18. Normal output mode circuit 2

Complementary output mode

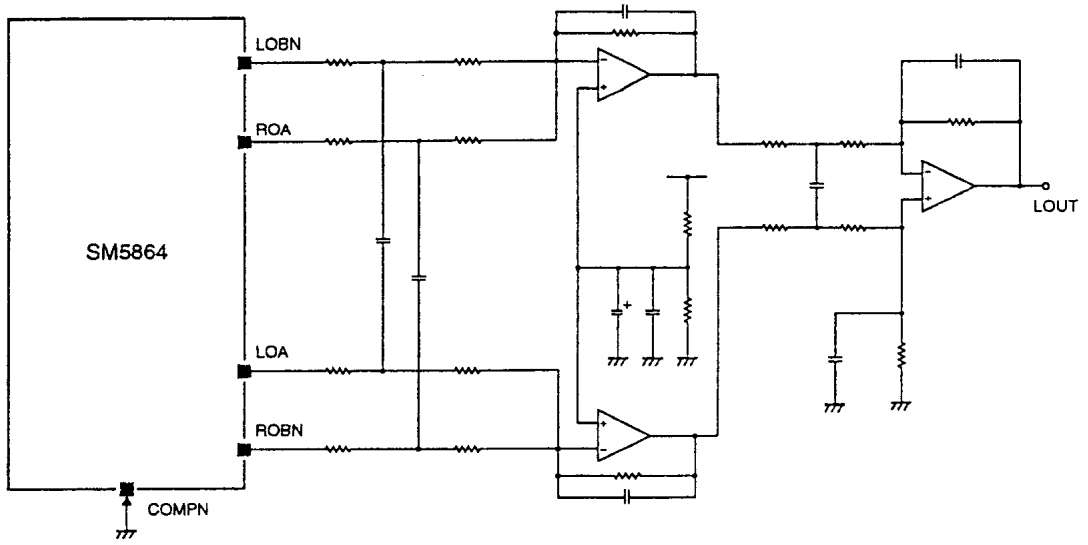


Figure 19. Complementary output mode circuit 1

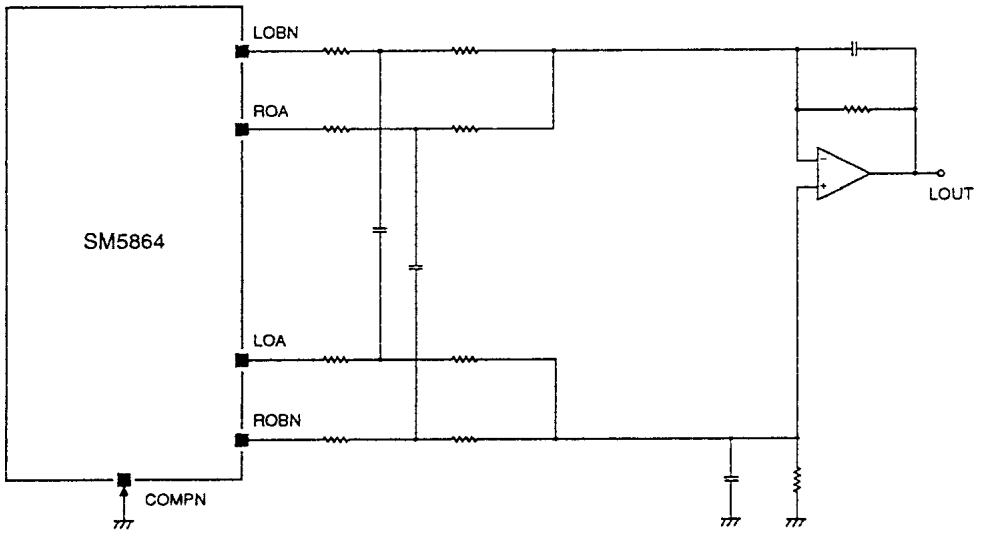


Figure 20. Complementary output mode circuit 2

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