NIPPON PRECISION CIRCUITS LTD.

SM5841C

Audio Multi-function Digital Filter

OVERVIEW

The SM5841C is a digital filter for digital audio, fabricated in Molybdenum-gate CMOS.

The SM5841C features 8-times oversampling, digital deemphasis, soft muting and a noise shaper. It can operate from a standard 5 V supply or a low-voltage 3.2 V supply.

The SM5841C is available in 18-pin plastic DIPs and 22-pin SOPs.

FEATURES

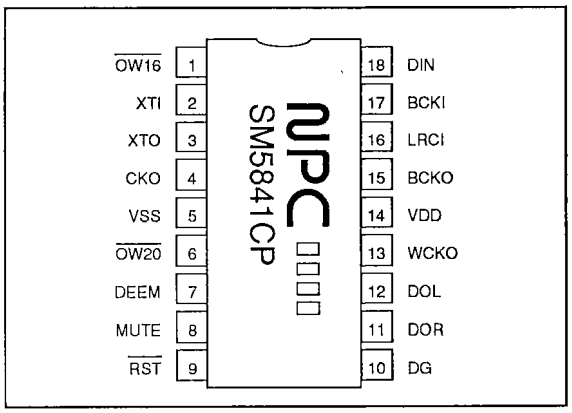
- Filter configuration
  - 2-channel, 8-times oversampling (interpolation) filter
  - 3-stage interpolation (69-tap + 13-tap + 9-tap)
  - 44.1 kHz IIR deemphasis filter for accurate gain and phase response
  - Overflow limiter
  - Crystal oscillator
- (fs = sampling frequency)
  - 0.20 ±0.03 dB passband (0 to 0.4535fs) ripple
  - 53 dB (min) stopband attenuation (0.5465fs to 7.4535fs)
  - Linear phase (zero group delay)
- Input/output
  - 16-bit serial data input (2s-complement, MSB-first)
  - 16-, 18- or 20-bit serial data output (2s-complement, MSB-first)
  - TTL-compatible
- 384fs system clock selectable
- Supply voltage
  - 5 V normal-voltage operation
  - 3.2 V low-voltage operation
- 18-pin plastic DIP or 22-pin SOP
- Molybdenum-gate CMOS process
- Filter functions
  - 1st-order noise shaper (ON/OFF selectable for 18-bit output)
  - Soft muting
  - Digital attenuation
  - Digital deemphasis (for 44.1 kHz)

APPLICATIONS

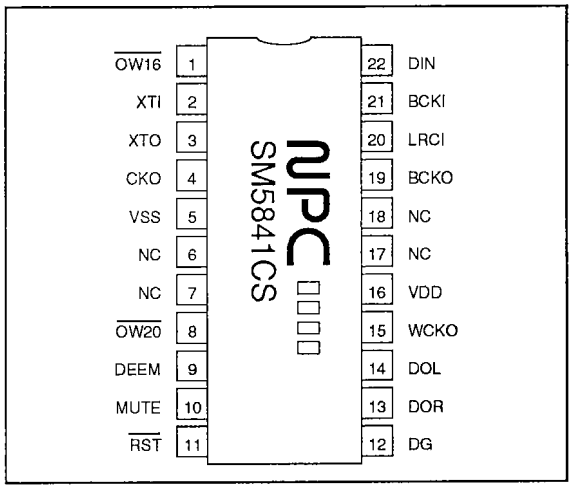
- CD playback systems
- PCM playback systems

PINOUTS

18-pin DIP



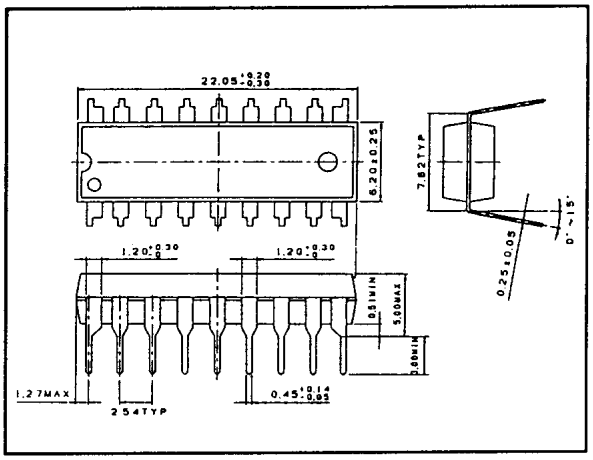
22-pin SOP



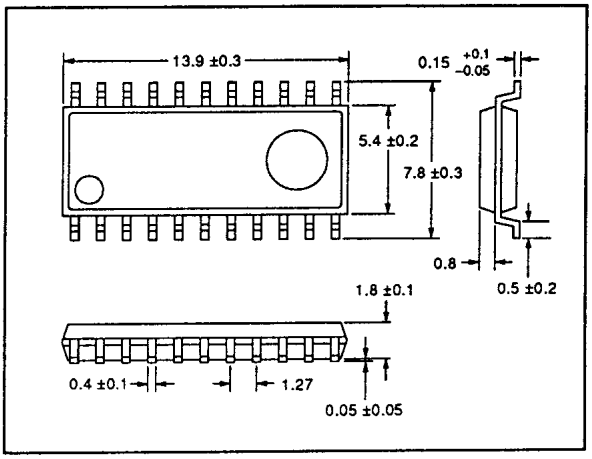
PACKAGE DIMENSIONS

Unit: mm

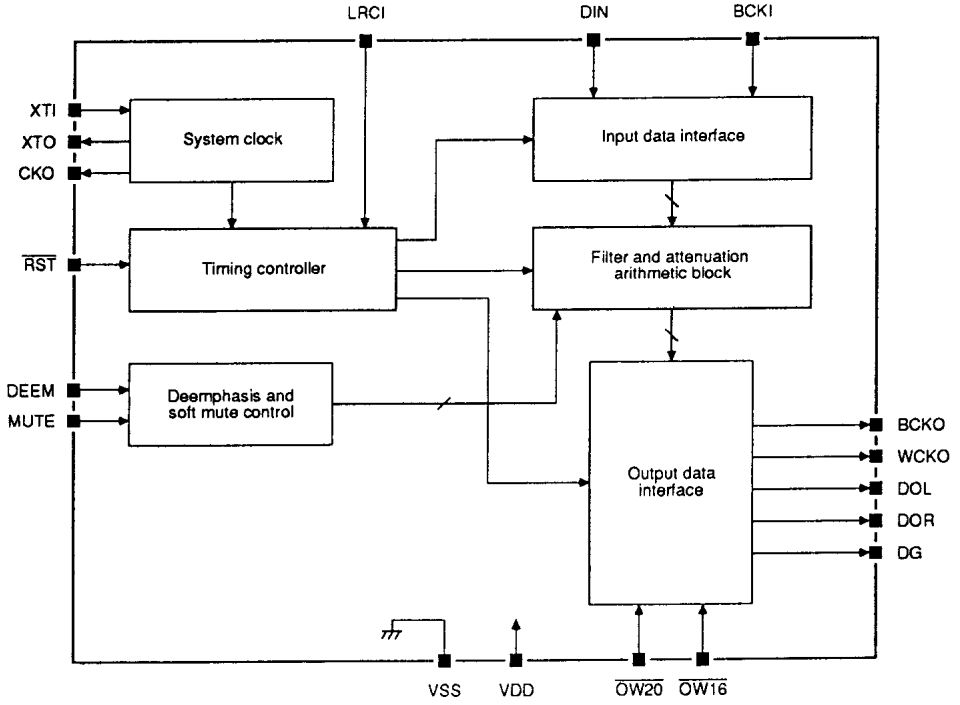
18-pin DIP



22-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th colspan="2">Number</th><th rowspan="2">Name</th><th rowspan="2">I/O</th><th rowspan="2">Description</th></tr>
<tr><th>SOP</th><th>DIP</th></tr>
<tr><td>1</td><td>1</td><td>$\overline{OW16}$</td><td>ip</td><td>Output word length select 1
<table>
<tr><th>$\overline{OW16}$</th><th>$\overline{OW20}$</th><th>Output word length (Noise shaper ON/OFF)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>18 bits (OFF)</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>16 bits (ON)</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>20 bits (ON)</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>18 bits (ON)</td></tr>
</table></td></tr>
<tr><td>2</td><td>2</td><td>XTI</td><td>i</td><td>Oscillator input connection</td></tr>
<tr><td>3</td><td>3</td><td>XTO</td><td>o</td><td>Oscillator output connection</td></tr>
<tr><td>4</td><td>4</td><td>CKO</td><td>o</td><td>Oscillator output clock (same frequency as XTI)</td></tr>
<tr><td>5</td><td>5</td><td>VSS</td><td></td><td>Ground</td></tr>
<tr><td>6</td><td>–</td><td>NC</td><td></td><td>No connection</td></tr>
<tr><td>7</td><td>–</td><td>NC</td><td></td><td>No connection</td></tr>
<tr><td>8</td><td>6</td><td>$\overline{OW20}$</td><td>ip</td><td>Output word length select 2
<table>
<tr><th>$\overline{OW16}$</th><th>$\overline{OW20}$</th><th>Output word length (Noise shaper ON/OFF)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>18 bits (OFF)</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>16 bits (ON)</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>20 bits (ON)</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>18 bits (ON)</td></tr>
</table></td></tr>
<tr><td>9</td><td>7</td><td>DEEM</td><td>ip</td><td>Deemphasis signal input. Deemphasis is OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>10</td><td>8</td><td>MUTE</td><td>ip</td><td>Mute signal input. Soft muting is OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>11</td><td>9</td><td>$\overline{RST}$</td><td>ip</td><td>System reset</td></tr>
<tr><td>12</td><td>10</td><td>DG</td><td>o</td><td>De-glitched output</td></tr>
<tr><td>13</td><td>11</td><td>DOR</td><td>o</td><td>Right-channel data output</td></tr>
<tr><td>14</td><td>12</td><td>DOL</td><td>o</td><td>Left-channel data output</td></tr>
<tr><td>15</td><td>13</td><td>WCKO</td><td>o</td><td>Output word clock</td></tr>
<tr><td>16</td><td>14</td><td>VDD</td><td></td><td>5 V supply</td></tr>
<tr><td>17</td><td>–</td><td>NC</td><td></td><td>No connection</td></tr>
<tr><td>18</td><td>–</td><td>NC</td><td></td><td>No connection</td></tr>
<tr><td>19</td><td>15</td><td>BCKO</td><td>o</td><td>Output bit clock</td></tr>
<tr><td>20</td><td>16</td><td>LRCI</td><td>ip</td><td>Input data sample rate (fs) clock</td></tr>
<tr><td>21</td><td>17</td><td>BCKI</td><td>ip</td><td>Input bit clock</td></tr>
<tr><td>22</td><td>18</td><td>DIN</td><td>ip</td><td>Data input</td></tr>
</table>

Note

i = input, ip = input with pull-up resistor, o = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	3.2 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	deg. C

DC Electrical Characteristics

Normal-voltage mode

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	V_{DD} = 5.0 V, f_{SYS} = 384fs = 19.3 MHz, no load	–	–	40	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}		–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –0.4 mA. See note 2.	2.5	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 1.6 mA. See note 2.	–	–	0.4	V
XTI HIGH-level input leakage current	I_{LH1}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input leakage current	I_{LL1}	V_{IN} = 0 V	–	10	20	µA
HIGH-level input leakage current	I_{LH2}	V_{IN} = V_{DD}. See note 1.	–	–	1.0	µA
LOW-level input current	I_{IL}	V_{IN} = 0 V. See note 1.	–	10	20	µA

Notes

1. Pins LRCI, DIN, BCKI, MUTE, DEEM, $\overline{OW16}$, $\overline{OW20}$ and $\overline{RST}$
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

Low-voltage mode

V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	V_{DD} = 3.4 V, f_{SYS} = 384fs = 18.5 MHz, no load	–	–	20	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}		–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –0.2 mA. See note 2.	2.5	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 0.8 mA. See note 2.	–	–	0.4	V
XTI HIGH-level input leakage current	I_{LH1}	V_{IN} = V_{DD}	–	–	12	µA
XTI LOW-level input leakage current	I_{LL1}	V_{IN} = 0 V	–	–	12	µA
HIGH-level input leakage current	I_{LH2}	V_{IN} = V_{DD}. See note 1.	–	–	1.0	µA
LOW-level input current	I_{IL}	V_{IN} = 0 V. See note 1.	–	–	12	µA

Notes

1. Pins LRCI, DIN, BCKI, MUTE, DEEM, $\overline{OW16}$, $\overline{OW20}$ and $\overline{RST}$
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

AC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C for normal-voltage operation.
V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C for low-voltage operation.
Typical values are measured at fs = 44.1 kHz.

System clock

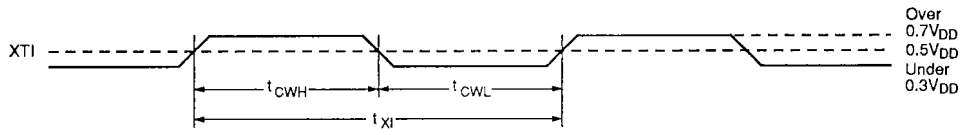
Crystal oscillator operation

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{MAX}	4.0	16.9	19.3	MHz

External clock input operation

Parameter	Symbol	Rating			Unit
		min	typ	max	
XTI HIGH-level clock pulsewidth	t_{CWH}	21.7	29.5	125	ns
XTI LOW-level clock pulsewidth	t_{CWL}	21.7	29.5	125	ns
XTI clock pulse time	t_{XI}	51.7	59.0	250	ns

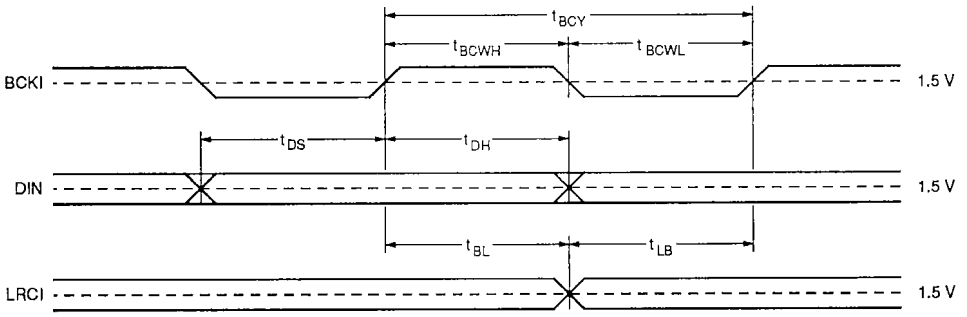
System clock timing waveform



Serial input timing (BCKI, DIN, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse period	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns

BCKI, DIN and LRCI input timing waveform



Reset timing

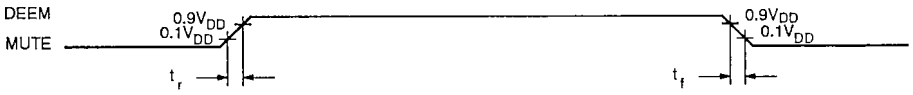
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level pulsewidth	t_{RST}	At power-on	1	–	–	µs
		At other times	50	–	–	ns

Control input timing (DEEM, MUTE)

Parameter	Symbol	Rating			Unit
		min	typ	max	
DEEM and MUTE rise time	t_r	–	–	100	ns
DEEM and MUTE fall time	t_f	–	–	100	ns

Control input timing waveform



Output timing

Normal-voltage mode

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	–	20	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	–	30	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = HIGH)	t_{sbH}	XTI falling edge to BCKO rising edge	10	–	60	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = LOW)	t_{sbH}	XTI rising edge to BCKO rising edge	10	–	60	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	–	20	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	–	20	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	–	20	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	–	20	ns

Note

All measurements with 15 pF load

Low-voltage mode

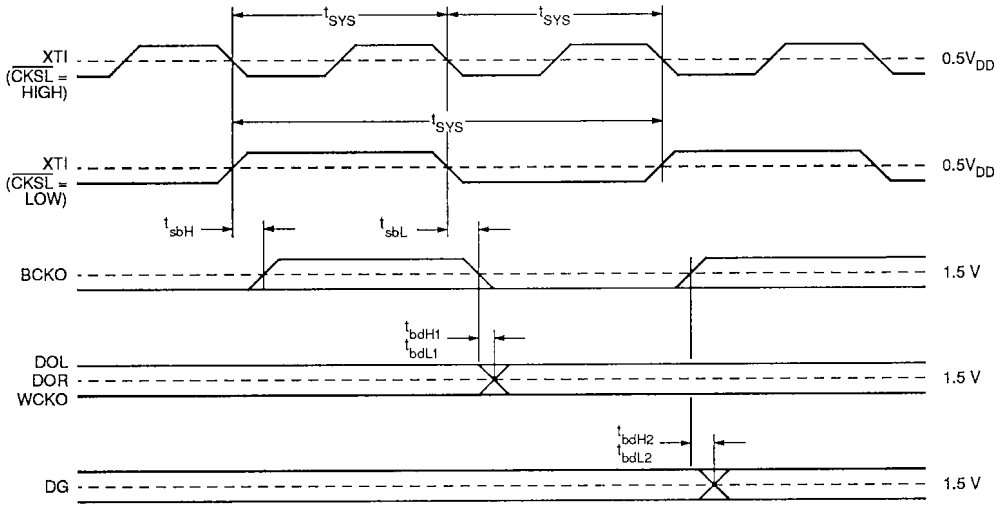
V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	–	30	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	–	45	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = HIGH)	t_{sbH}	XTI falling edge to BCKO rising edge	10	–	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	100	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = LOW)	t_{sbH}	XTI rising edge to BCKO rising edge	10	–	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	100	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	–	30	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	–	30	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	–	30	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	–	30	ns

Note

All measurements with 15 pF load

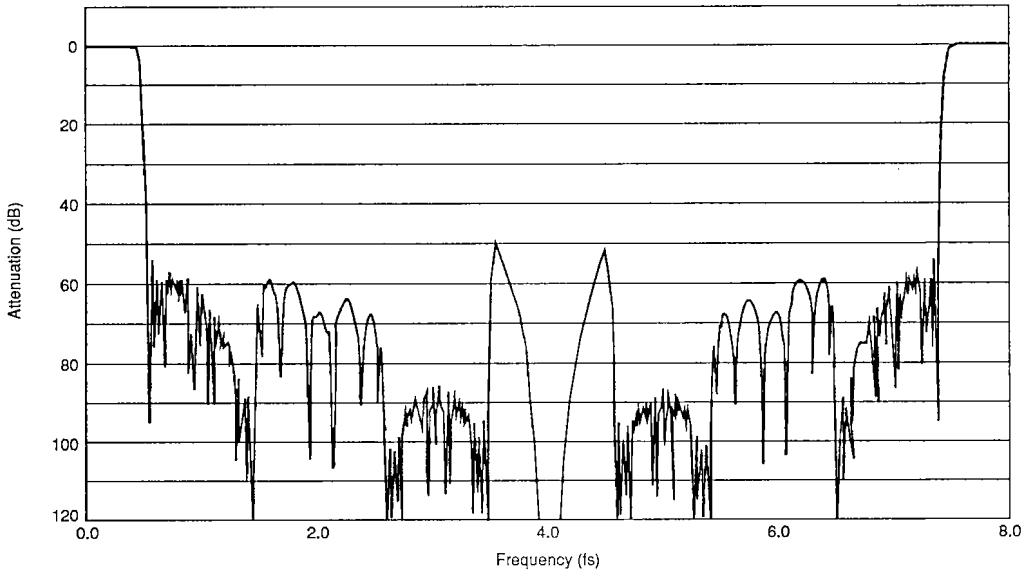
Output timing waveform



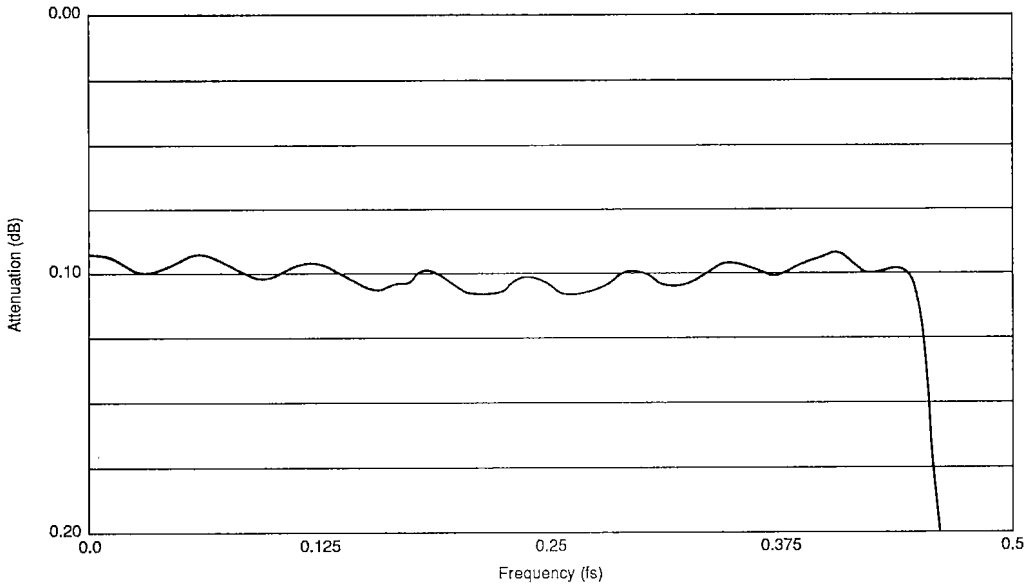
Filter Characteristics

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	0.03
Stopband attenuation	0.5465fs to 3.4535fs	21.4 to 152 kHz	53	–	–
	3.4535fs to 4.5465fs	152 to 201 kHz	50	–	–
	4.5465fs to 7.4535fs	201 to 328 kHz	53	–	–

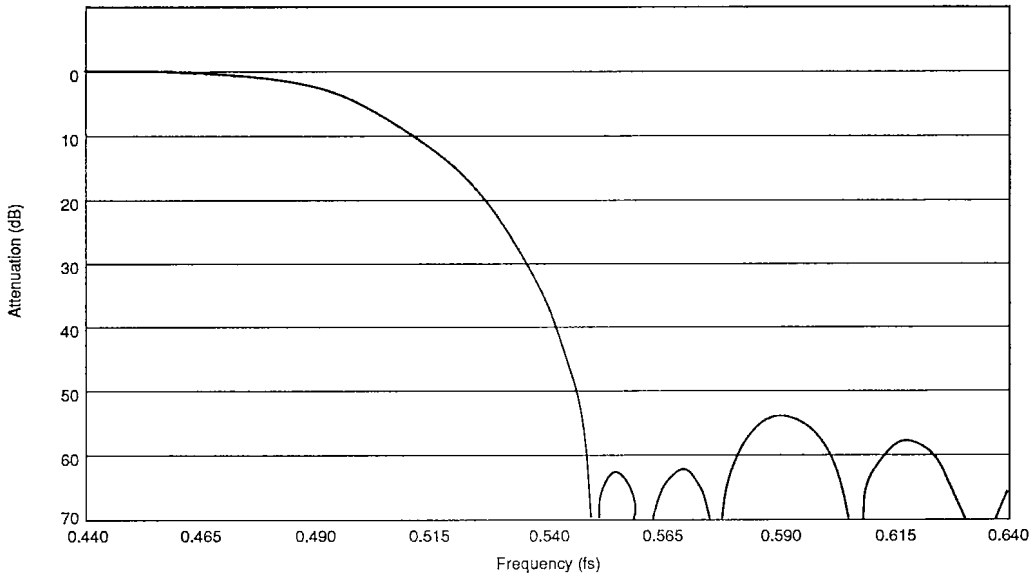
8fs filter frequency characteristic (Deemphasis OFF)



8fs filter passband characteristic (Deemphasis OFF)



8fs filter band-transition characteristic (Deemphasis OFF)



Deemphasis filter

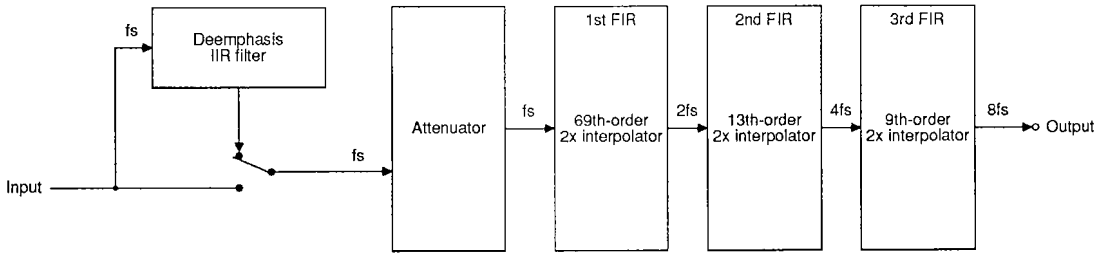
Parameter		Rating at fs = 44.1 kHz
Passband bandwidth (kHz)		0 to 20.0
Deviation from ideal characteristics	Attenuation (dB)	−0.05 to 0.15
	Phase, θ (°)	−1 to 1.5

Note

These are the maximum deviations from a 1 kHz input signal with 0 dB attenuation and 0° phase ideal characteristic.

FUNCTIONAL DESCRIPTION

SM5841C Arithmetic Block



Oversampling (Interpolation)

The SM5841C performs oversampling using a three-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two, giving an overall interpolation factor of eight. Sampling noise components are attenuated by the interpolation filter to greater than 53 dB in the 0.5465fs to 7.4535fs stopband.

Digital Deemphasis

The deemphasis filter is in cascade with the oversampling filters. It is implemented using an IIR filter, and reproduces the deemphasis gain and phase characteristics more faithfully than conventional analog deemphasis filters. Deemphasis is enabled when DEEM is HIGH, and disabled when DEEM is LOW.

Soft Mute

The oversampled output can be muted using a built-in digital attenuator controlled by the MUTE pin. Muting is ON when MUTE is HIGH, and OFF when MUTE is LOW.

When MUTE is HIGH, the maximum attenuation coefficient (DATT) 127 is loaded into the temporary-storage register and the attenuation slowly changes to ∞ dB in unit steps.

When MUTE is LOW, the maximum attenuation coefficient (DATT) 0 is loaded into the temporary-storage register and the attenuation slowly changes to 0 dB in unit steps.

Both the left and right channels are attenuated simultaneously by an amount

$$\text{Attenuation} = 20 \times \log_{10} (1 - \text{DATT}/127)\ \text{dB}$$

where DATT is the contents of the attenuation register. When DATT = 127, the attenuation is infinite (mute function).

If MUTE changes level before the maximum/minimum level is reached, the gain ramps in the direction of the latest set level.

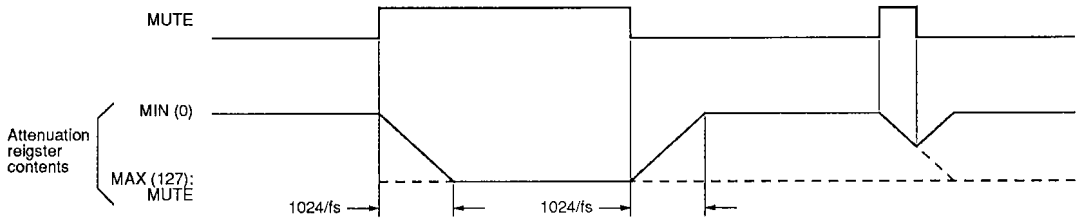


Figure 1. Attenuation level changes

The time taken to increase the attentuation from 0 (DATT = 1) to ∞ dB (DATT = 127) is approximately 1024/fs, which is approximately 23.2 ms at fs = 44.1 kHz.

System Clock (XTI, XTO, CKO)

The system clock operates at 384fs. The clock can be generated either externally (input on XTI) or internally (crystal oscillator between XTI and XTO). The clock is output on CKO.

Table 1. System clock

System clock frequency	Clock input	Internal operating frequency	Serial output clock frequency
384fs	External clock on XTI OR Crystal oscillator between XTI and XTO	128fs	192fs

Audio Data Input (DIN, BCKI, LRCI)

The input is in 16-bit, 2s-complement, MSB-first, serial data format.

Input timing

Serial input data on DIN is clocked into an SIPO register on the rising edge of the BCKI bit clock, and then converted into parallel data.

The SIPO output data for each channel is latched into the left-channel/right-channel input register on the rising/falling edge of LRCI.

The timing of the arithmetic and output circuits is independent of the input timing. Accordingly, phase differences between LRCI, BCKI and XTI do not cause incorrect operation, and data input clock jitter does not generate jitter in the output clock.

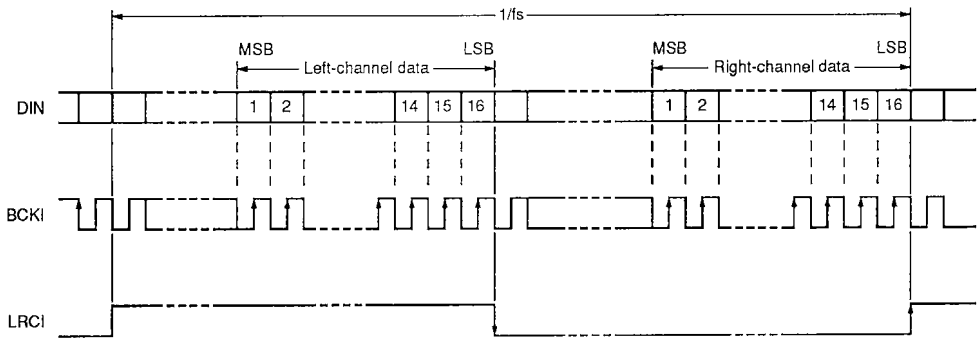


Figure 2. Audio data input timing

Data Output (DOL, DOR, BCKO, WCKO, DG, $\overline{OW16}$, $\overline{OW20}$)

The output is in 8fs L/R alternating, 2s-complement, MSB-first serial format. The output word length is 16-, 18- or 20-bit selectable using $\overline{OW16}$ and $\overline{OW20}$.

The output timing is shown in table 2.

Table 2. Output timing

Parameter	Symbol	Rating
Bit clock rate	t_B	1/192fs
Data word length	t_{DW}	$24t_B$

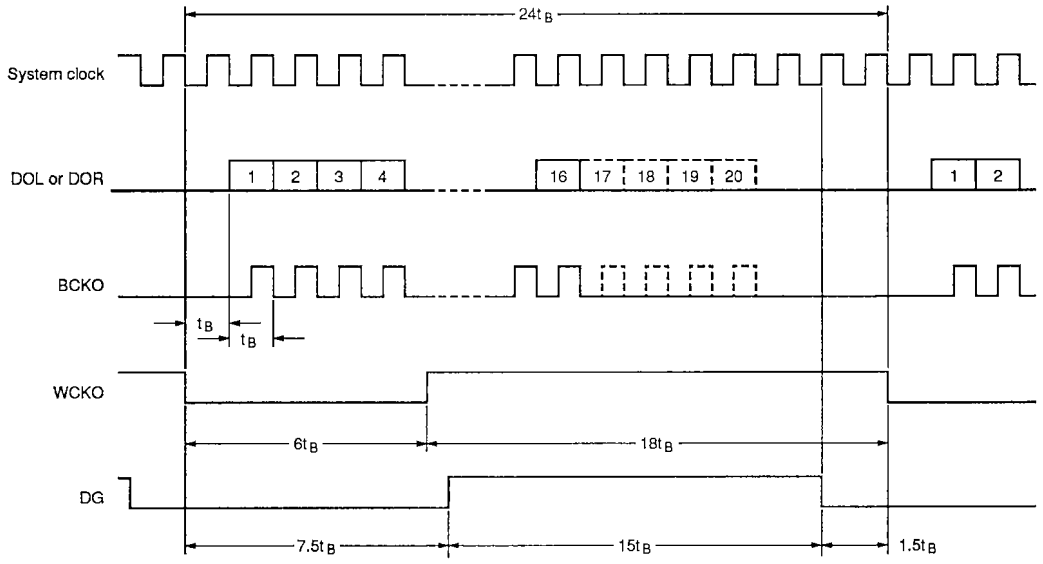


Figure 3. Data output timing

Note
In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

System Reset

The SM5841C must be reset at power-ON and when $\overline{CKSL}$ changes state by applying at LOW-level pulse on $\overline{RST}$.

At system reset, the arithmetic and output timing counters are reset on the next LRCI start edge after XTI has stablilized.

A power-ON reset pulse can be applied from a controlling microprocessor, or by connecting a 300 pF capacitor between $\overline{RST}$ and VSS for systems where XTI and LRCI stablilize simultaneously. For others systems that do not use a microcontroller, XTI and LRCI must stabilize before $\overline{RST}$ goes HIGH. A larger capacitor can be used to ensure that this occurs.

If the system clock becomes corrupted or develops jitter such that the timing increases above ±3/8 × (LRCI clock frequency), then the internal timing will automatically reset on the next LRCI start edge. This timing re-synchronization can generate an output click noise.

Output Muting

When $\overline{RST}$ goes LOW, DOL and DOR go LOW, immediately muting the output words. Muting is released and timing re-synchronized on the third LRCI rising edge after $\overline{RST}$ goes HIGH. The BCKO and WCKO clock outputs do not stop.

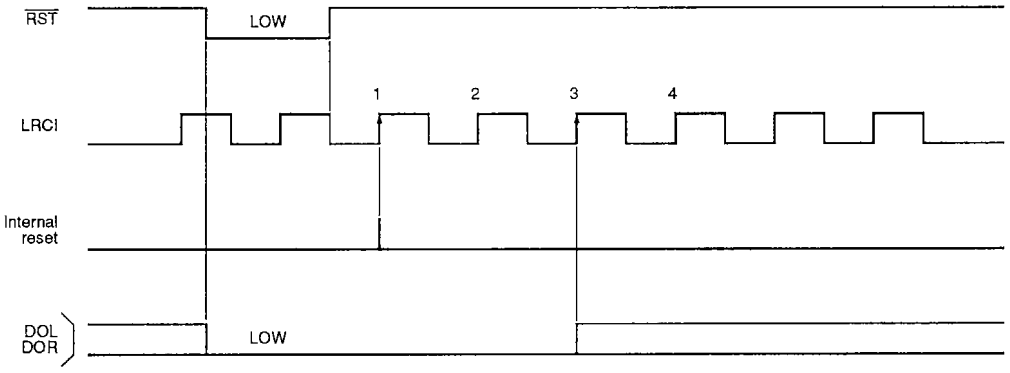


Figure 4. System reset timing and output muting

TIMING DIAGRAMS

Input Timing (DIN, BCKI, LRCI)

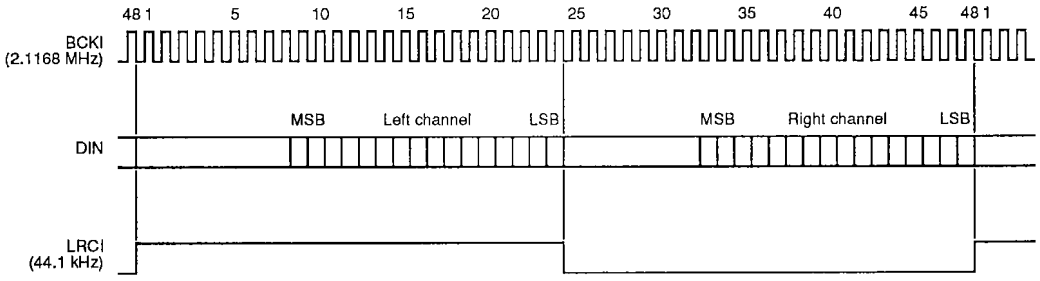


Figure 5. Input timing 1

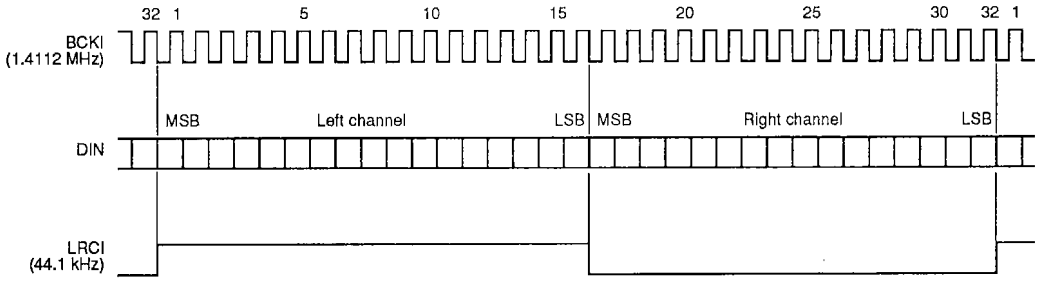


Figure 6. Input timing 2

Output Timing (DOL, DOR, BCKO, WCKO, DG)

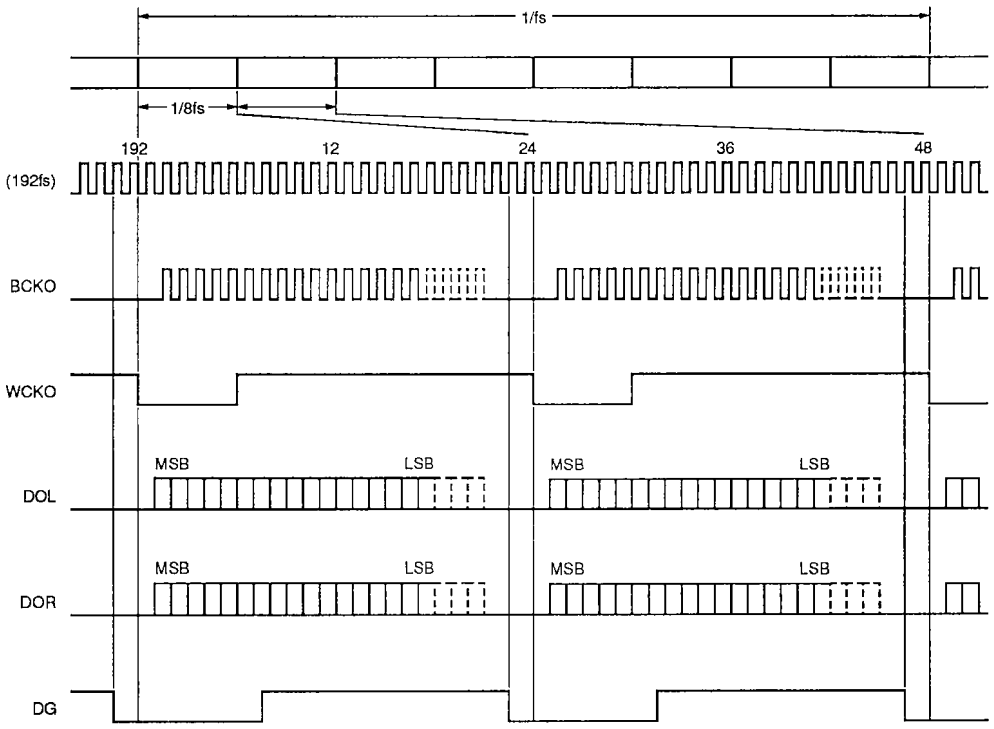


Figure 7. Output timing

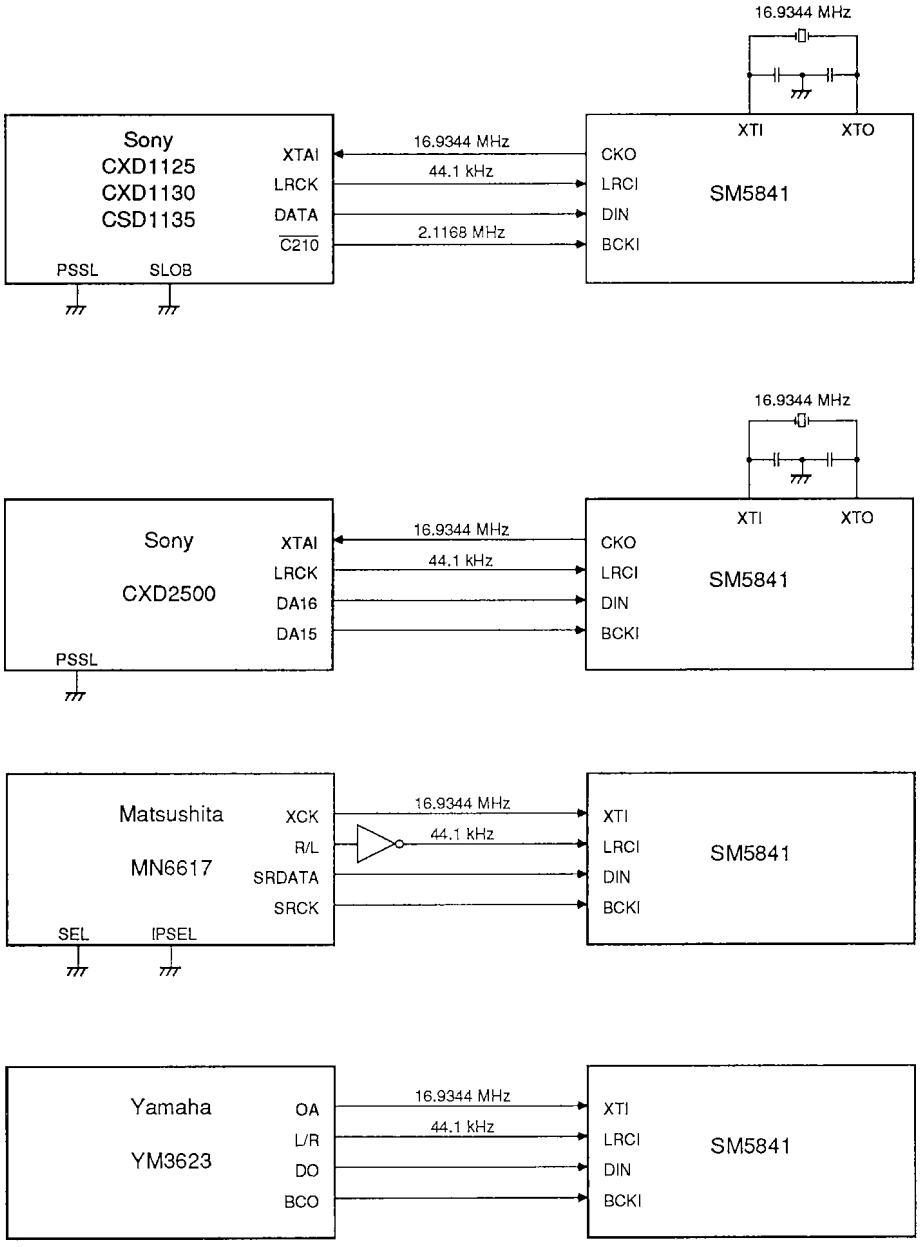
Note

The length of the output word, and hence the number of DOL and DOR bits and BCKO pulses per word, varies depending on the state of $\overline{\text{OW16}}$ and $\overline{\text{OW20}}$.

APPLICATION CIRCUITS

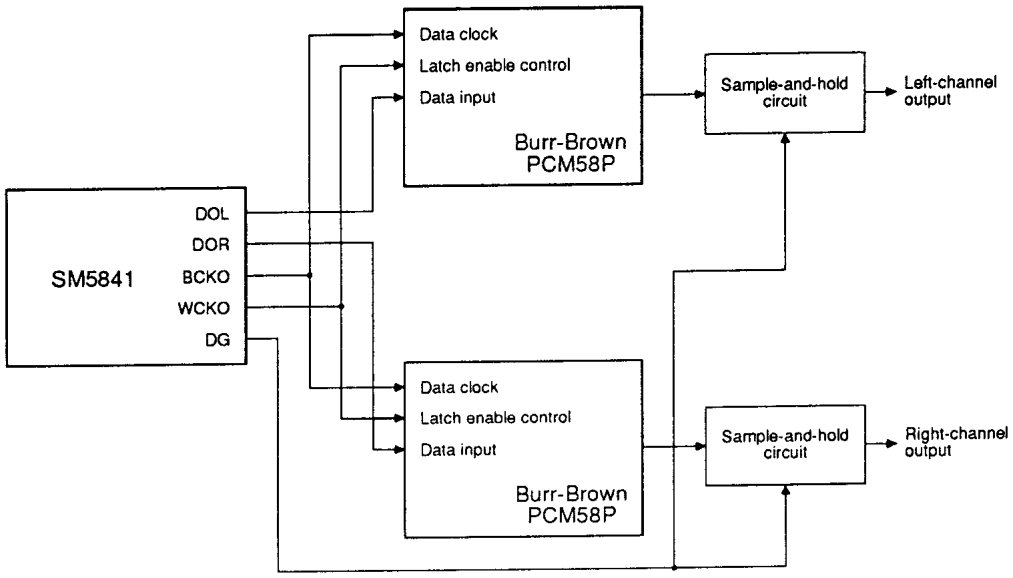
The following interface circuits all use the signal formats shown in the previous section. The timing relationships, however, need to be determined separately for each circuit.

Input Interface Circuits



Output Interface Circuits

18-bit dual D/A converter (8fs L/R alternating output mode)



NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

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