■ OVERVIEW

The SM5828B is a variable-length 8-bit shift register fabricated using NPC's original molybdenum-gate CMOS technology. The external input pins of the IC allow 1 to 128-step shift register settings. The shift clock with the maximum frequency of 20 MHz ensures high-speed operation.
As static registers are used, data is retained even when the shift clock is stopped.

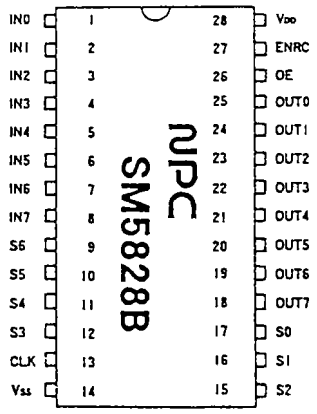
■ FEATURES

- 1 to 128-step settings
- 8-bit (1-byte) parallel input/output
- Static registers
- Selection between circulation and non-circulation
- Maximum operating clock frequency 20 MHz
- Supply voltage 5 V ±0.5 V
- Input/output TTL compatible
- 28-pin DIP (plastic, ceramic)
- Molybdenum-gate CMOS construction

■ PACKAGE TYPES

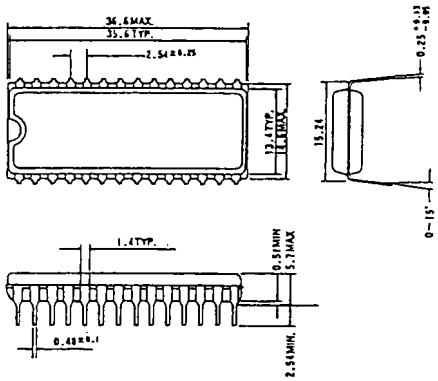
Type	Package
SM5828BP	28-pin plastic DIP
SM5828BC	28-pin ceramic DIP

■ PINOUT TOP VIEW

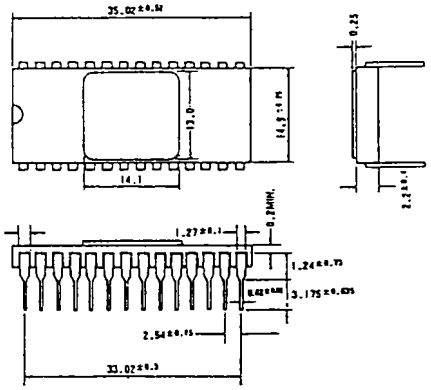


■ PACKAGE DIMENSIONS (Unit: mm)

• Plastic (SM5828BP)

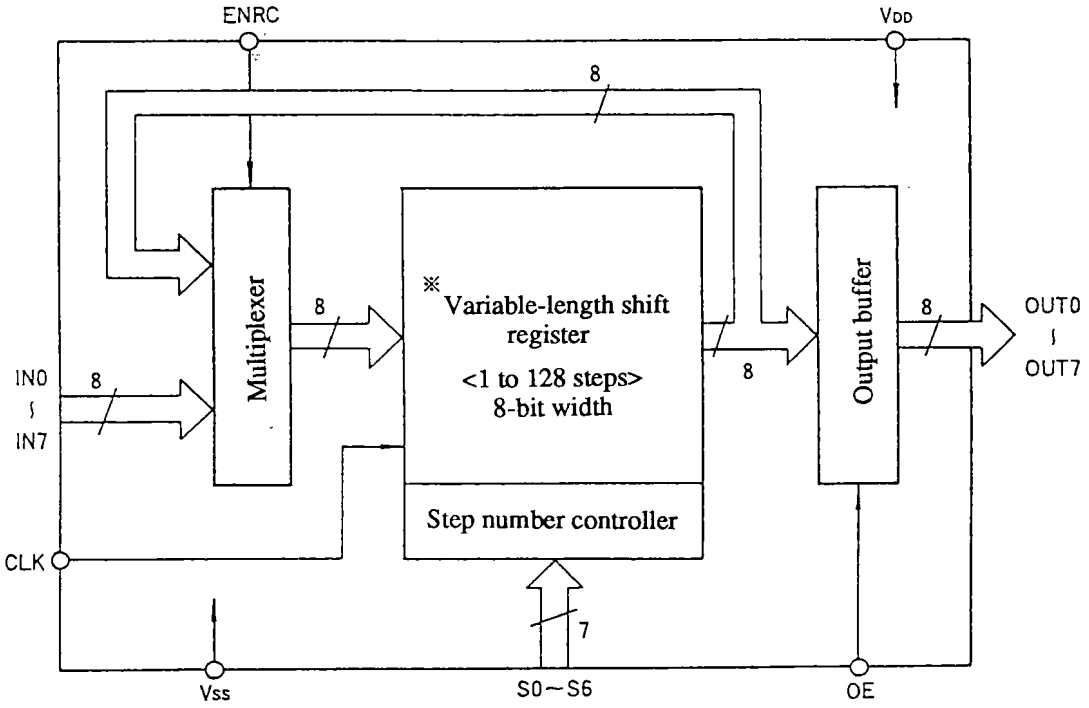


• Ceramic (SM5828BC)



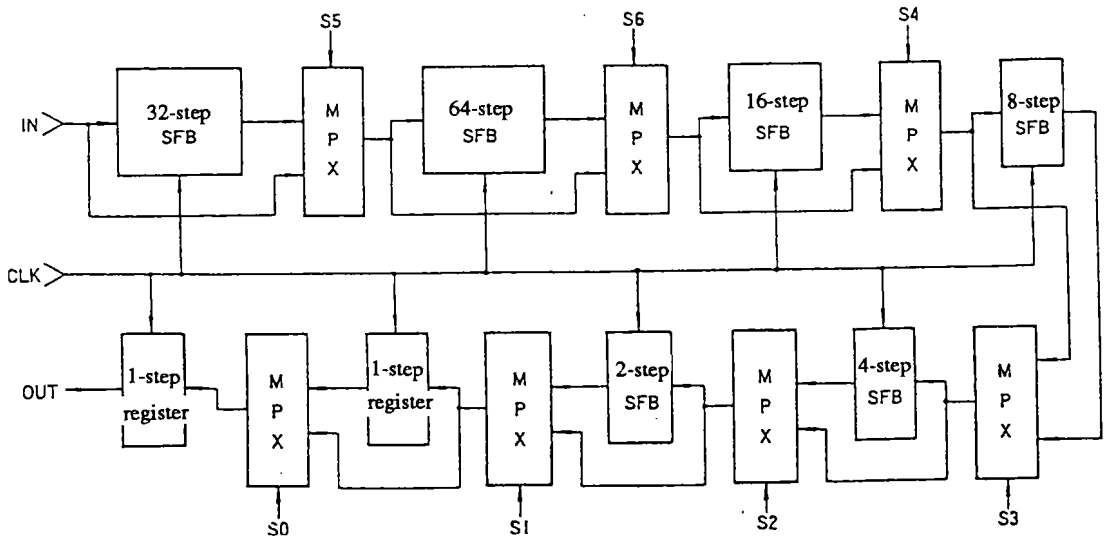
* The SM5828BC guarantees high reliability.

■ BLOCK DIAGRAM



* Internal configuration of the variable-length shift register

The figure below shows the configuration of the variable-length shift register. According to the setting of S0 to S6, the multiplexer selects the output of each shift register block, realizing 1 to 128-step shift registers. The last 1-step register is always used.



MPX: Multiplexer

SFB : Shift register block

■ PIN DESCRIPTION

No	Name	Description
1	IN0	Data input (0)
2	IN1	Data input (1)
3	IN2	Data input (2)
4	IN3	Data input (3)
5	IN4	Data input (4)
6	IN5	Data input (5)
7	IN6	Data input (6)
8	IN7	Data input (7)
9	S6	Data length select (6)
10	S5	Data length select (5)
11	S4	Data length select (4)
12	S3	Data length select (3)
13	CLK	Clock input
14	V_{SS}	Ground
15	S2	Register length select (2)
16	S1	Register length select (1)
17	S0	Register length select (0)
18	OUT7	Data output (7)
19	OUT6	Data output (6)
20	OUT5	Data output (5)
21	OUT4	Data output (4)
22	OUT3	Data output (3)
23	OUT2	Data output (2)
24	OUT1	Data output (1)
25	OUT0	Data output (0)
26	OE	Output enable
27	ENRC	Circulation and non-circulation control
28	V_{DD}	Power supply (5 ± 0.5 V)

Note All input pins have pull-up resistors.
All output pins are in tristate.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−40 to 125	°C
Power dissipation	P_W	750	mW
Soldering temperature	T_{SLD}	255	°C
Soldering time	t_{SLD}	10	Sec

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Unit
Supply voltage	V_{DD}	4.5 to 5.5	V
Operating temperature (SM5828P)	T_{OPRP}	−20 to 70	°C
Operating temperature (SM5828C)	T_{OPRC}	−30 to 85	°C

■ DC CHARACTERISTICS

(SM5828BP ... Ta = -20 to 70 °C, VDD = 4.5 to 5.5 V, Vss = 0 V
SM5828BC... Ta = -30 to 85 °C, VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted.)

Paramete	Pin	Symbol	Condition	Rating			Unit	Remarks
				MIN	TYP	MAX		
Current consumption at standby	V_{DD}	I_{ST}	V_{DD} - 5.5V		0.01	100	μA	
Current consumption during operation	V_{DD}	I_{DD}	Note			100	mA	See Figure 2.
Input voltage	*1	V_{IH}		2.4			V	
		V_{IL}				0.5		
Output voltage	*2	V_{OH}	I_{OH} = – 0.4mA	2.5			V	
		V_{OL}	I_{OL}= 1.6mA			0.4		
Input current	*1	I_{IL}	V_{IN} = 0V		7	20	μA	
Input leak current	*1	I_{LH}	V_{IN} = V_{DD}			1	μA	
Output Hi-Z current	*2	I_{ZH}	V_{OUT} = V_{DD}			5	μA	
		I_{ZL}	V_{OUT} = 0V			5		

(Pin type)

* 1	ENRC, IN0 to IN7, S0 to S6, CLK, OE
* 2	OUT1 to OUT7

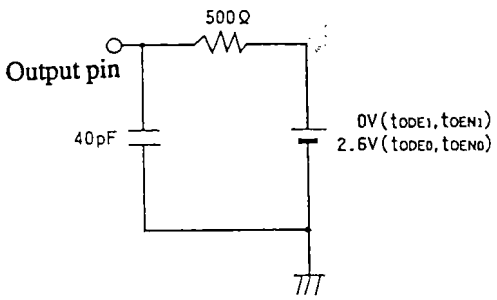
Note) Clock frequency f_{CLK} = 20 MHz, OE pin = 0 V
Clock input voltage V_{IH} = 2.4 V, V_{IL} = 0.5 V

■ AC CHARACTERISTICS

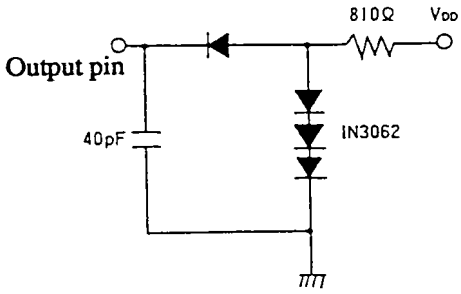
(VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted)

Paramete	Pin	Symbol	Condition	BP type (–20 to 70°C) BC type(–20 to 85°C)			BC type (–30 to 70°C)			Unit	Remarks
				MIN	TYP	MAX	MIN	TYP	MAX		
Clock frequency	CLK	f_{CLK}	V_{IH} = 2.4V, V_{IL} = 0.5V			20			20	MHz	
Clock rise time	CLK	t_{cr}				100			100	nsec	
Clock fall time	CLK	t_{cf}				100			100	nsec	
Clock pulse width	CLK	t_{WH}		20			20			nsec	
Input setup time	IN0 to 7 ENRC	t_{S1}	Register length: LR = 1 to 16 steps Figure 1	60			55			nsec	Figure 1
		t_{S2}	Register length: LR = 17 to 128 steps Figure 1	45			40			nsec	Figure 1
	SO to 6	t_{S3}		80			80			nsec	
Input hold time	IN0 to 7 ENRC	t_{H1}		0			0			nsec	
	S0 to 6	t_{H2}		10			10			nsec	
Output enable delay time	OUT 0 to 7	t_{OEN}	Load condition 1 (Note 1)			40			35	nsec	Figure 3
Output disable delay time	OUT 0 to 7	t_{ODE}	Load condition 1 (Note 1)			40			35	nsec	Figure 3
Output data delay time	OUT 0 to 7	t_D	Load condition 2 (Note 2)			45			40	nsec	Figure 3

(Note 1) Load condition 1



(Note 2) Load condition 2



■ REGISTER STEP SETTING

Set the number of register steps by using the register length select pins S0 to S6.

L=64•(S6)+32•(S5)+16•(S4)+8(S3)+4•(S2)+2•(S1)+(S0)+1

Step	S6	S5	S4	S3	S2	S2	S0
128	1	1	1	1	1	1	1
127	1	1	1	1	1	1	0
126	1	1	1	1	1	0	1
125	1	1	1	1	1	0	0
.				.			
.				.			
.				.			
66	1	1	0	0	0	0	1
65	1	1	0	0	0	0	0
.				.			
.				.			
.				.			
3	0	0	0	0	0	1	0
2	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0

Note)

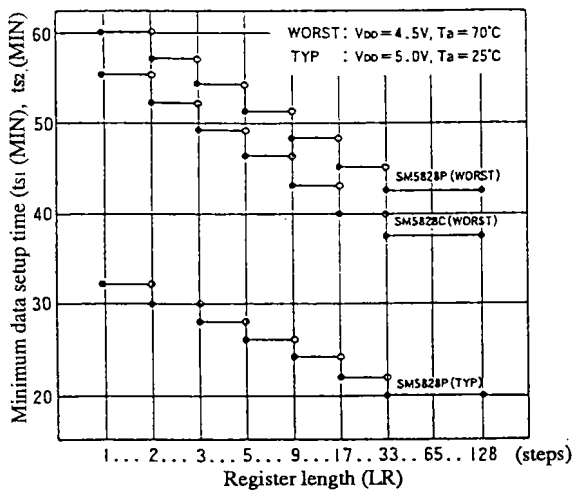
1. 1 ... High or Open,
   0 .... Low
2. S0 to S6 pins have internal pull-up resistors.

■ INPUT/OUTPUT CONTROL

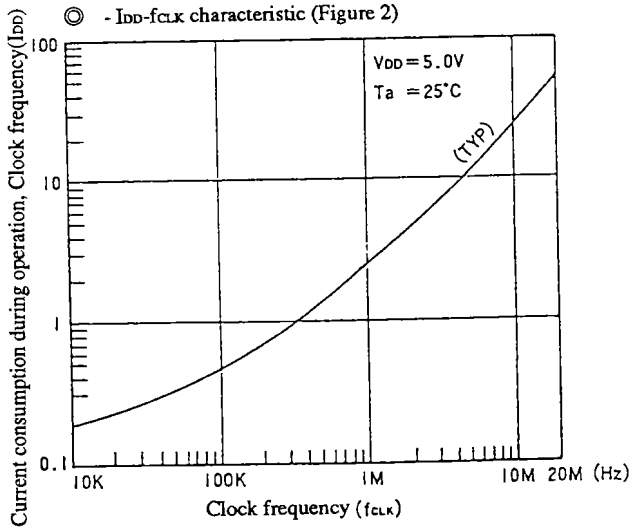
Input			Shift register (internal)	Output
ENRC	CLK	OE		OUT0 to OUT7
X	X	0	–	Hi–Z
X	X	1	–	ENABLE
1	⎍	X	Circulation	–
0	⎍	X	No circulation	–

■ TYPICAL CHARACTERISTICS

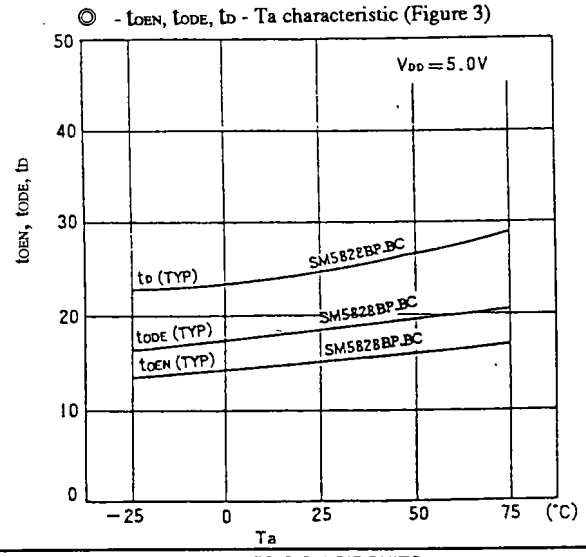
◎ t_{s1}, t_{s2} (MIN) — LR characteristic (Figure 1)



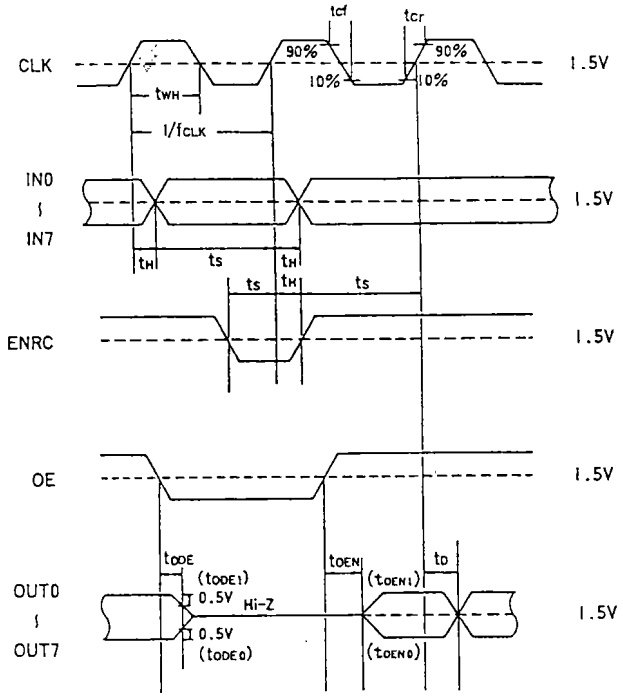
◎ - I_{DD}-f_{CLK} characteristic (Figure 2)



◎ - t_{OEN}, t_{ODE}, t_D - Ta characteristic (Figure 3)



■ TIMING CHART



■ TYPICAL APPLICATION (Block diagram of a 16-bit FIR digital filter using the SM5828B)