

NPC DISCONTINUED PRODUCT

SM5807

NIPPON PRECISION CIRCUITS LTD. FOLD OVER SAMPLING DIGITAL FILTER FOR DIGITAL AUDIO

■ GENERAL DESCRIPTION

SM5807 is a four fold over sampling digital filter for low end digital audio system, using the molybdenum gate C-MOS process developed solely by NPC.

This LSI has two channel FIR filters, and the pass-band ripple is less than $\pm 0.05\text{dB}$, stop band attenuation is more than 50dB. The input and output datas are 16-bit serial, so the circuit system can be small.

■ FEATURES

• FILTER STRUCTURE

- Four fold over sampling
- Two channel filter
- Cascaded linear phase FIR filter (61st+13th order)
- On chip overflow limiter
- On chip quartz oscillation circuit
- Buffer output for XT input clock

• FILTER CHARACTERISTICS

Filter characteristics	SM5807DP, DS	SM5807EP, ES, FP, FS
Pass band ripple(0~20kHz)	Within $\pm 0.05\text{dB}$	Within $\pm 0.05\text{dB}$
[Pass band attenuation]	[Within $\pm 0.05\text{dB}$]	[0~0.1dB]
Stop band attenuation(24.1kHz~)	More than 50dB	More than 45dB

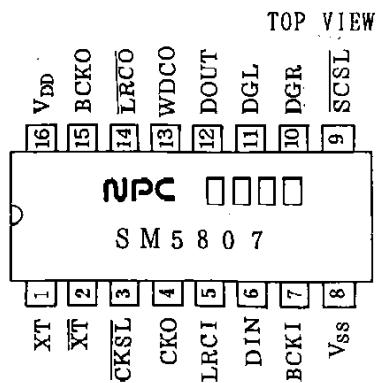
-Linear Phase (There is no group delay distortion.)

• INPUT/OUTPUT

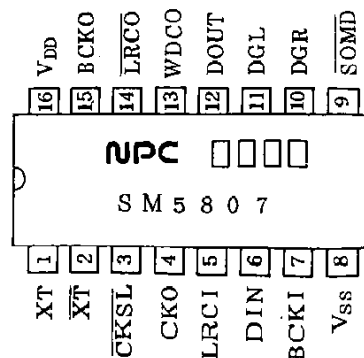
- 16 bit serial input/output
(2's complement code, MSB first)
- TTL compatible
- Interface for 2DACs(F type)
- Power supply voltage: $5\text{V} \pm 0.5\text{V}$
- 16 pin plastic DIP/SOP
- Molybdenum gate C-MOS process

■ PIN CONFIGURATION

• D, E Type



• F Type



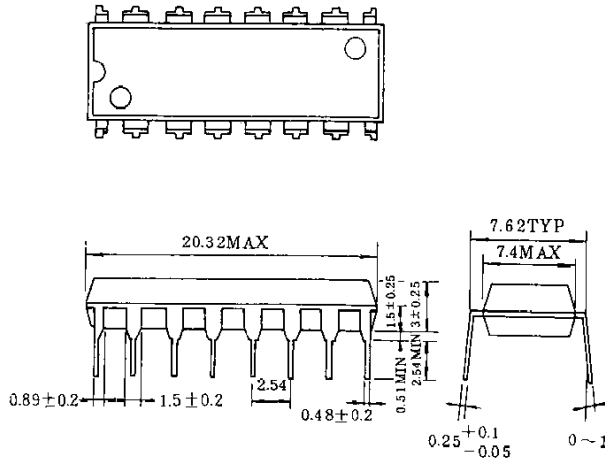
■ PACKAGE TYPE

TYPE	PACKAGE
SM5807DP, EP, FP	16 Pin plastic DIP
SM5807DS, ES, FS	16 Pin plastic SOP

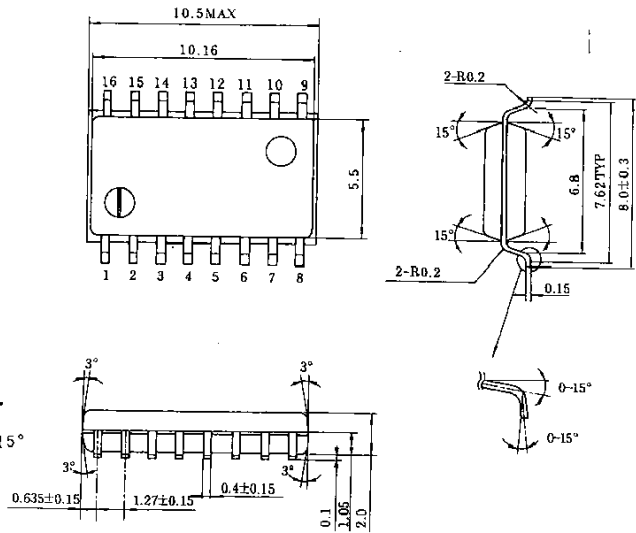
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PACKAGE DIMENSION (UNIT:mm)

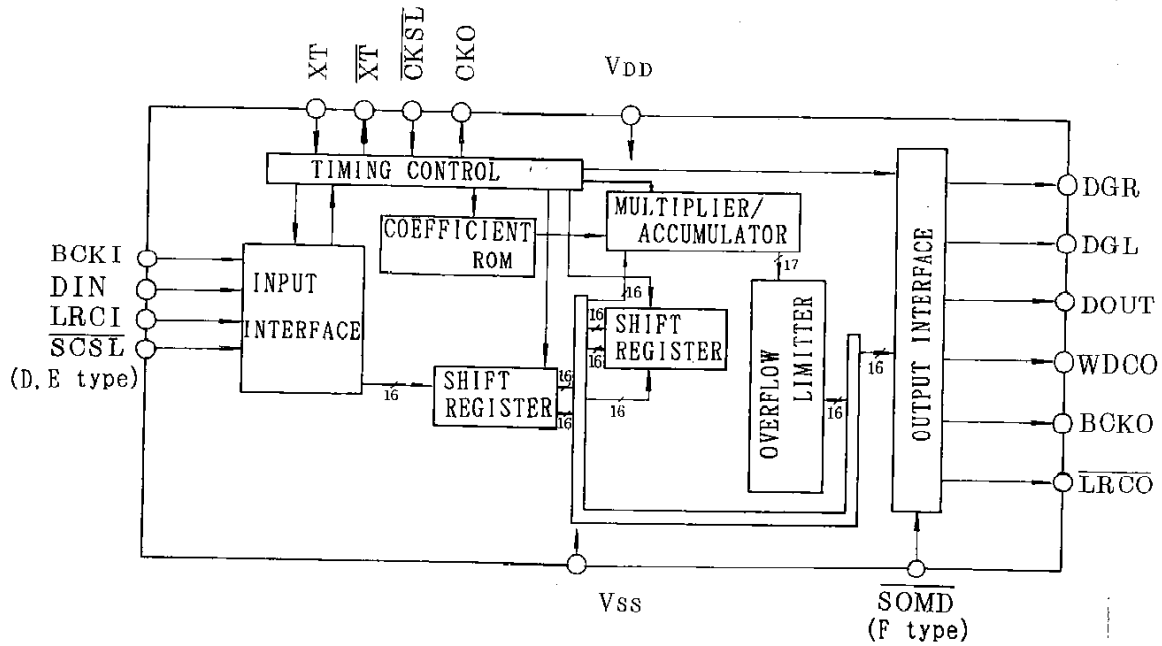
・DIP



・SOP



BLOCK DIAGRAM



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■ FILTER CHARACTERISTICS
(THEORITICAL VALUE)

1. SM5807 DP, DS

(frequency:0~88.2kHz)

ITEM	CHARACTERISTICS
PASS BAND	0~20kHz
STOP BAND	More than 24.1kHz
PASS BAND RIPPLE	Within $\pm 0.05\text{dB}$
STOP BAND ATTENUATION	More than 50dB

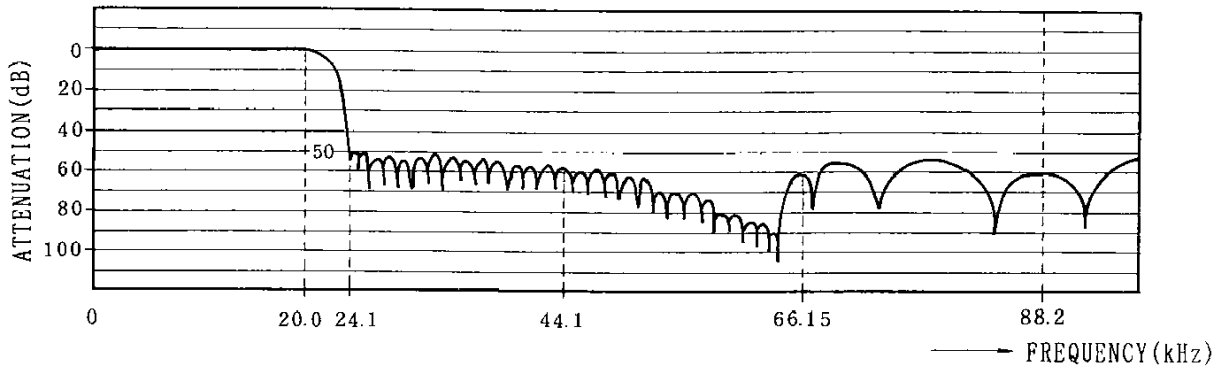


Fig.1 Characteristics of frequency domain

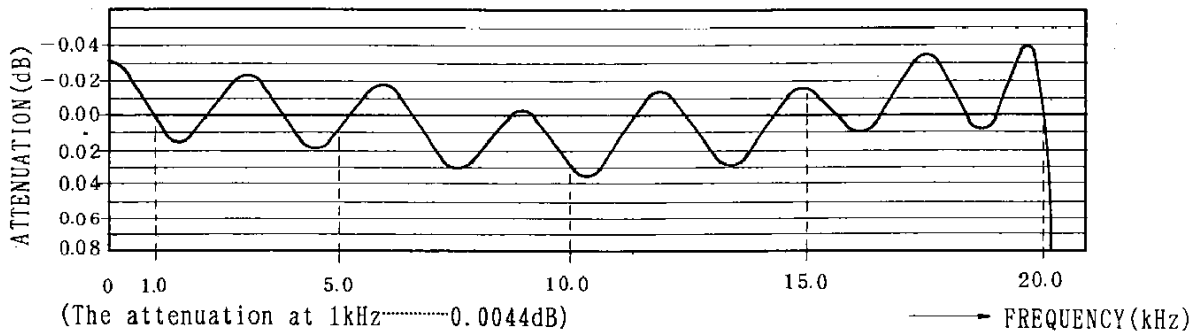


Fig.2 Pass band

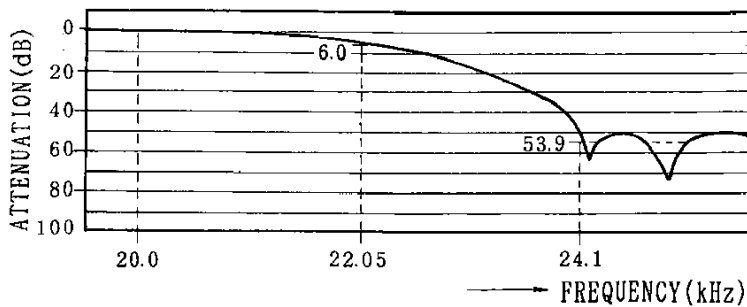


Fig.3 The domain between pass band and stop band

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1. SM5807 EP, ES, FP, PS

(frequency:0~88.2kHz)

ITEM	CHARACTERISTICS	
PASS BAND	0~20kHz	
STOP BAND	More than 24.1kHz	
PASS BAND RIPPLE	Within ± 0.05 dB	
STOP BAND	24.1~40kHz	More than 45dB
ATTENUATION	40.0kHz~	More than 50dB

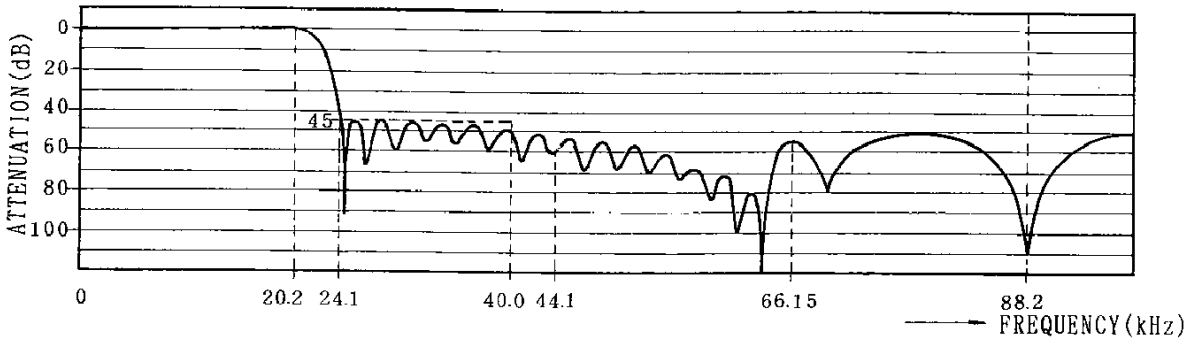


Fig. 4 Characteristics of frequency domain

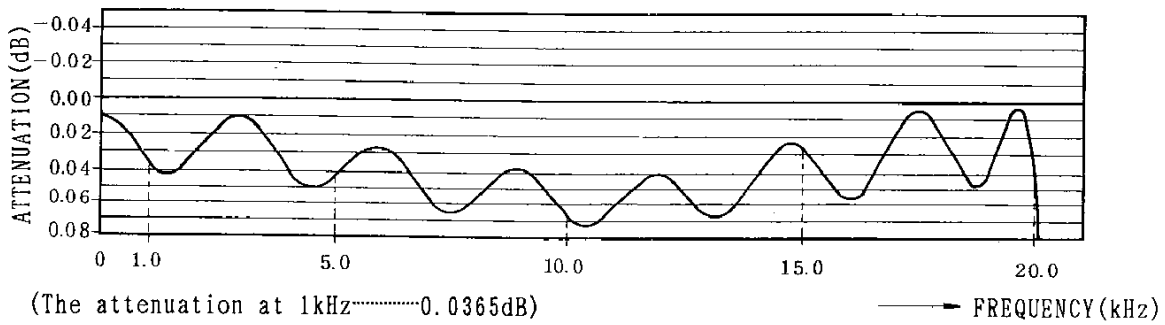


Fig. 5 Pass Band

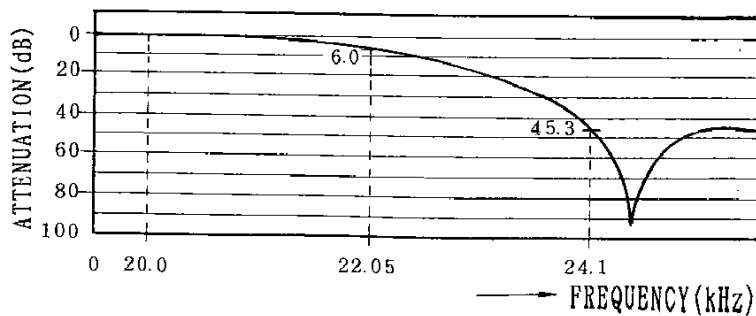


Fig. 6 The domain between pass band and stop band

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■ PIN DESCRIPTION

No.	NAME	I/O	DESCRIPTION
1	XT	I	Input for oscillator or external clock input
2	XT	O	Output for oscillator, No connect at using external clock
3	CKSL	Ip	"H"-----XT input clock is 16.9344MHz or 17.2872MHz(F type-----only 16.9344MHz) "L"-----XT input clock is 8.4672MHz or 8.6436MHz (F type-----only 8.4672MHz)
4	CKO	O	Buffer out of XT clock
5	LRCI	Ip	Lch,Rch Synchronizing clock
6	DIN	Ip	Serial data input
7	BCKI	Ip	Timing clock for serial input data
8	Vss	—	Ground
9	SCSL	Ip	"H"-----System clock→192fs
	(D,E)		"L"-----System clock→196fs (fs:Sampling frequency)
	SOMD	Ip	"H"-----Output interface for 1 DAC (Same as D,E type)
	(F)		"L"-----Output interface for 2 DACs
10	DGR	O	Rch deglitch signal(176.4kHz)
11	DGL	O	Lch deglitch signal(176.4kHz)
12	DOUT	O	Serial data output
13	WDCO	O	Output timing control clock(352.8kHz)
14	LRCO	O	Output timing control clock(176.4kHz)
15	BCKO	O	Timing clock for serial output data(8.4672kHz or 8.6436kHz) (F type-----only8.4672MHz)
16	V _{DD}	—	Supply voltage(+5V)

NOTE) I :Input terminal

Ip:Input terminal with pull-up resistance

O :Output terminal

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PRODUCT****■ ABSOLUTE MAXIMUM RATINGS**(V_{SS}=0V)

ITEM	SYMBOL	LIMITS	UNIT
SUPPLY VOLTAGE	V _{DD}	-0.3 ~ 7.0	V
INPUT VOLTAGE	V _{IN}	-0.3 ~ V _{DD} +0.3	V
STORAGE TEMPERATURE	T _{STG}	-40 ~ 125	°C
POWER DISSIPATION	P _W	250	mW
SOLDERING TEMPERATURE	T _{SLD}	255	°C
SOLDERING TIME	t _{SLD}	10	Sec

■ RECOMMENDATORY OPERATING CONDITION(V_{SS}=0V)

ITEM	SYMBOL	CONDITION	UNIT
SUPPLY VOLTAGE	V _{DD}	4.5 ~ 5.5	V
OPERATING TEMPERATURE	T _{OPR}	-20 ~ 70	°C

■ ELECTRIC CHARACTERISTICS· DC CHARACTERISTICS (T_a=-20~70°C, V_{DD}=4.5~5.5V, V_{SS}=0V)

ITEM	TERMINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION	V _{DD}	I _{DD}	V _{DD} =5V			20	mA
INPUT VOLTAGE (1)	XT	V _{IH1}		0.7V _{DD}			V
		V _{IL1}				0.3V _{DD}	V
INPUT VOLTAGE (2)	(*1)	V _{IH2}		2.4			V
		V _{IL2}				0.5	V
OUTPUT VOLTAGE	(*2)	V _{OH}	I _{OH} =-0.4mA	2.5			V
		V _{OL}	I _{OL} =1.6mA			0.4	V
INPUT LEAK CURRENT	XT	I _{LH}	V _{IN} =V _{DD}		5	15	μA
		I _{LL}	V _{IN} =0V		5	15	μA
	(*1)	I _{LH}	V _{IN} =V _{DD}			1.0	μA
INPUT CURRENT	(*1)	I _{IL}	V _{IN} =0V		10	20	μA

< TERMINAL >

*1	CKSL, LRC1, DIN, BCK1, SCSL (D, E Type), SOMD (F Type)
*2	CKO, LRCO, BCKO, WDCO, DOUT, DGL, DGR

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AC CHARACTERISTICS

1. XT TERMINAL

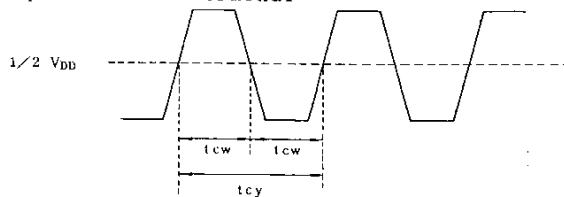
a. In case of crystal oscillation ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Oscillating frequency	f_{osc}			20	MHz	CKSL=H
				10	MHz	CKSL=L

b. In case of clock input to XT terminal ($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Width of clock pulse	t_{cw}	50		1000	nSec	CKSL=L
		25		500	nSec	CKSL=H
Cycle time of clock pulse	t_{cy}	100		2000	nSec	CKSL=L
		50		1000	nSec	CKSL=H

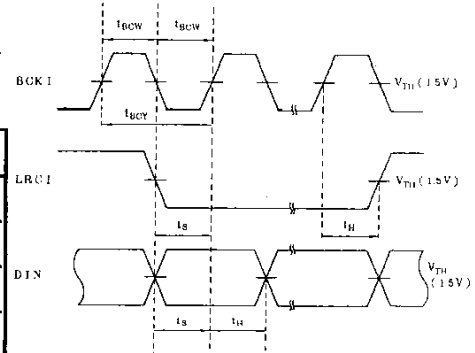
Input pulse to XT terminal



2. INPUT TIMING (DIN, BCKI, LRCI)

($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

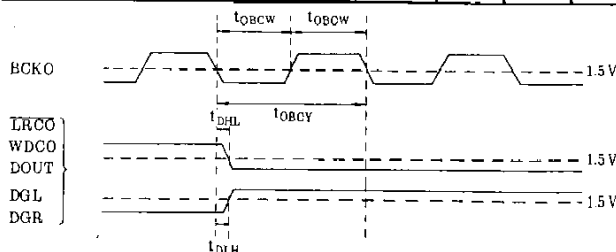
ITEM	SYMBOL	MIN	TYP	MAX	UNIT
BCKI, Pulse width	t_{bcw}	100			nSec
BCKI, Cycle time	t_{bcy}	200			nSec
DIN, LRCI, Set up time	t_s	75			nSec
DIN, LRCI, Hold time	t_h	75			nSec



3. OUTPUT TIMING

($T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
BCKO, Pulse width	t_{obcw}	40			nSec	
BCKO, Cycle time	t_{obcy}	100			nSec	
Output delay time	t_{dHL}	0		25	nSec	LRCO, WDCO, DOUT, DGL, DGR
	t_{dLH}			25	nSec	



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■ FUNCTION

(1) SYSTEM CLOCK

D, E type $\overline{\text{SCSL}}=\text{H}$ or OPEN.....192fs(8.4672MHz)
 $\overline{\text{SCSL}}=\text{L}$196fs(8.6436MHz) } fs:Sampling frequency(44.1kHz)
 F typeonly 192fs(8.4672MHz)

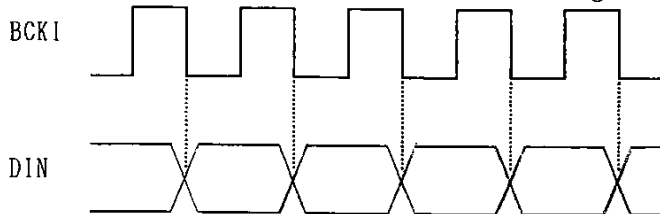
* Generating clock.....Crystal oscillation or external clock

CKSL	D, E Type($\overline{\text{SCSL}}=\text{H}$ or OPEN) F Type		D, E Type($\overline{\text{SCSL}}=\text{L}$)	
	H or open	L	H or open	L
XT/XT input frequency	384fs= 16.9344MHz	192fs= 8.4672MHz	392fs= 17.2872MHz	196fs= 8.6436MHz
CKO output	↑	↑	↑	↑
Internal system clock	192fs= 8.4672MHz	↑	196fs= 8.6436MHz	↑

(2) SERIAL INPUT(DATA & TIMING CLOCK)

The serial data input timing is raising edge of BCKI. So the input serial data must be changed at falling edge of BCKI.

And the input data is latched to the internal register by LRCl.



(3) INPUT DATA FORMAT

The input data format is 2's complement and MSB first.

(4) INTERNAL CALCULATION

The internal calculation starts at raising edge of LRCl.

(5) SERIAL OUTPUT(DATA & TIMING CLOCK)

The Lch/Rch datas are out from DOUT terminal alternately. So the 1 DAC interface system can be available. (D, E type & $\overline{\text{SOMD}}=\text{H}$ of F type)

And using F type($\overline{\text{SOMD}}=\text{L}$) and 2DACs, the in-phase conversion is possible.

(Refer to 12 page.)

The output timing clock is out from BCKO terminal and the output data changes at falling edge of BCKO clock, so the data input timing to DAC is raising edge of BCKO.

BCKO=8.4672MHz(At $\overline{\text{SCSL}}=\text{H}$ or open of D, E type/F type)

BCKO=8.6436MHz(At $\overline{\text{SCSL}}=\text{L}$ of D, E type)

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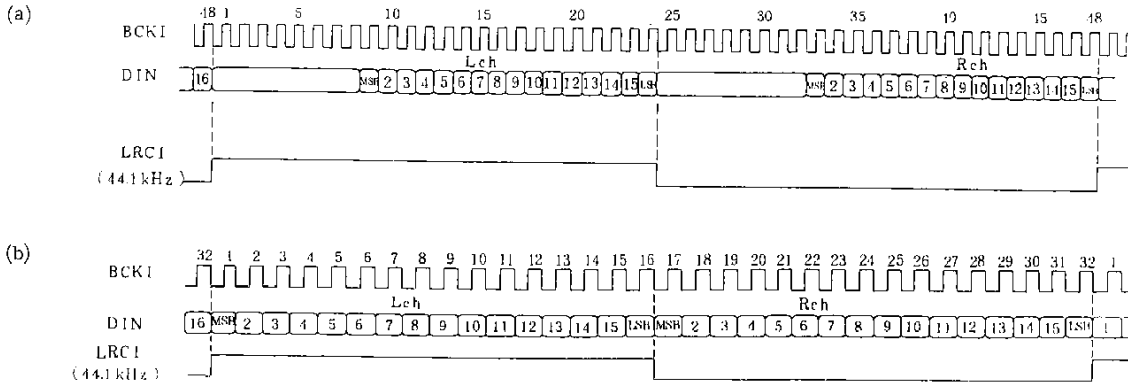
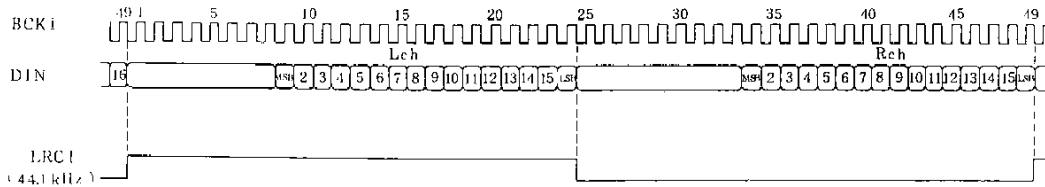
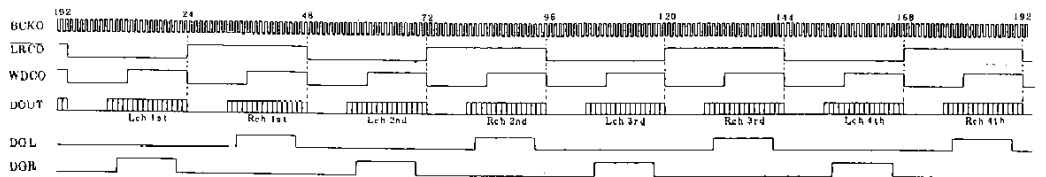
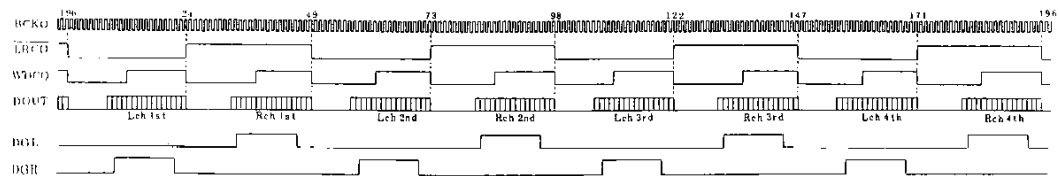
(6) OUTPUT DATA FORMAT

The output data format is 2's complement and MSB first.

(7) DEGLITCH SIGNAL

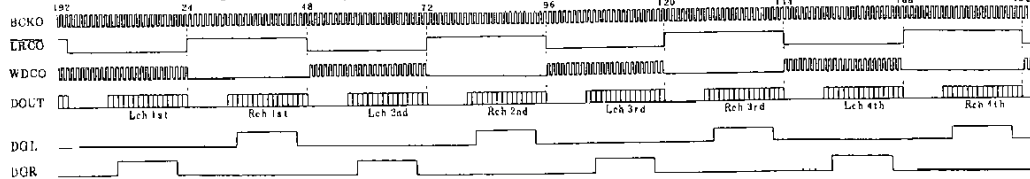
DGL.....Lch deglitch signal 176.4kHz(Duty 25%)

DGR.....Rch deglitch signal 176.4kHz(Duty 25%)

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PRODUCT****■ TIMING CHART****1. INPUT****(1) INPUT TIMING 1 (D, E Type; \overline{SCSL} =H or OPEN & F Type)****(2) INPUT TIMING 2 (D, E Type; \overline{SCSL} =L)****2. OUTPUT****(1) OUTPUT TIMING 1 (D, E Type; \overline{SCSL} =H or OPEN & F Type \overline{SOMD} =H or OPEN)****(2) OUTPUT TIMING 2 (D, E Type; \overline{SCSL} =L)**

The output cycle of WDCO is not constant.

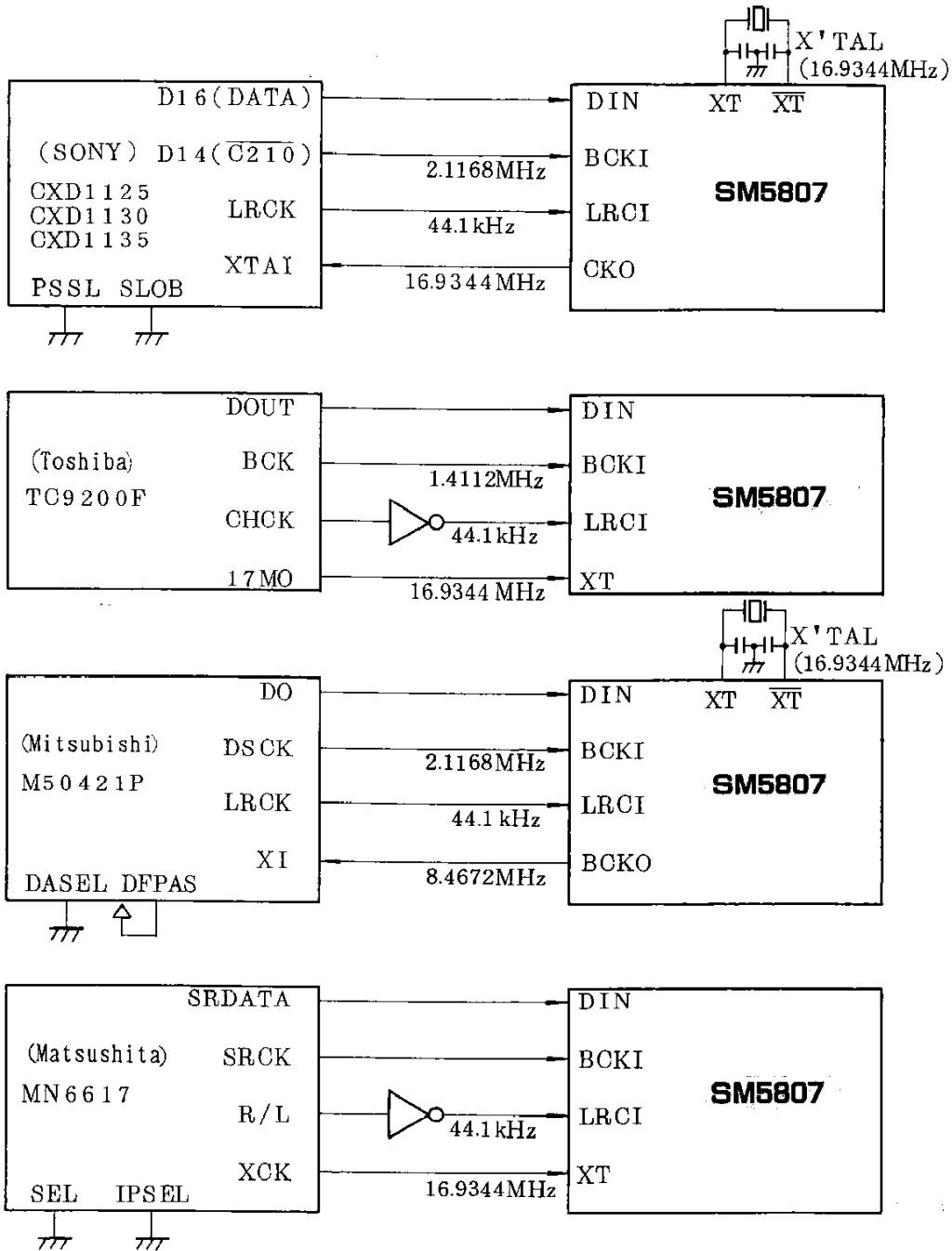
But the DGL, DGR cycles are constant. (176.4kHz, Duty 25%)

(3) OUTPUT TIMING 3 (F Type; \overline{SOMD} =L)

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■ TYPICAL APPLICATION

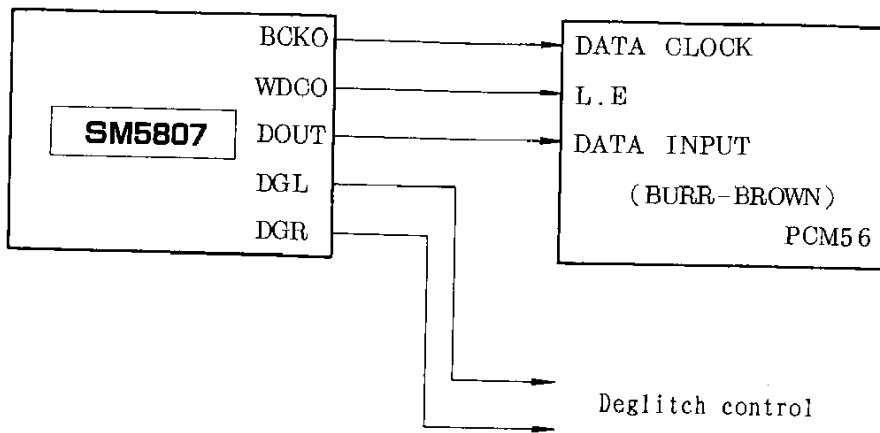
1. INPUT

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2. OUTPUT

(1) 1DAC (D, E Type & F Type; SMD=H or OPEN)



(2) 2DACs (F Type; SMD=L)

