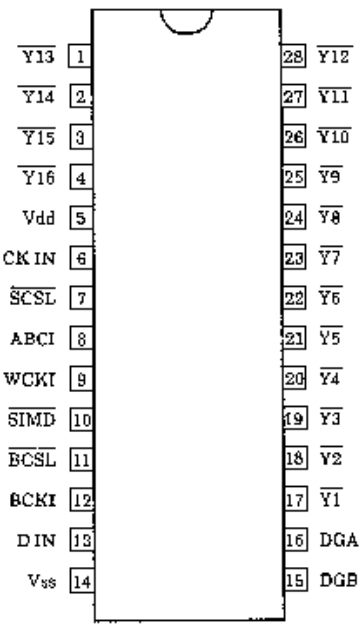
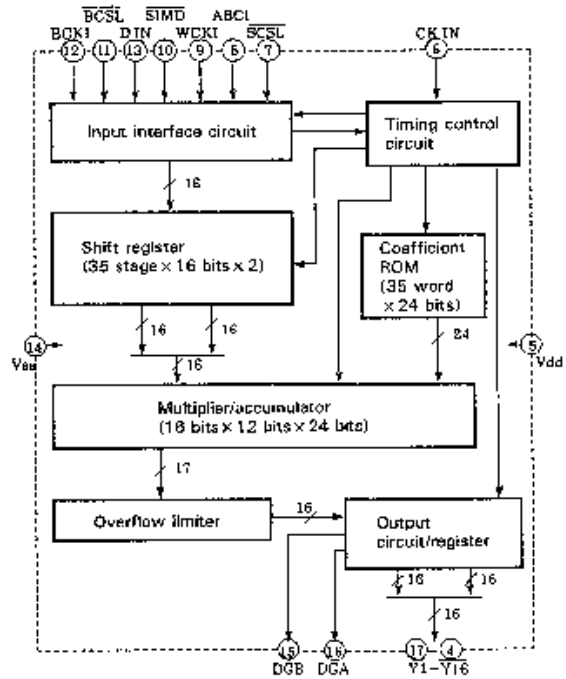
SM5806P (Digital Filter)

(1) External diagram

SM5806P



(2) Internal block diagram



(3) Pin functions

SM5806P

Pin No.	Pin Name	I/O	Function
1	$\overline{Y13}$	O	Parallel data inverted output (inversion BIT 13)
2	$\overline{Y14}$	O	Parallel data inverted output (inversion BIT 14)
3	$\overline{Y15}$	O	Parallel data inverted output (inversion BIT 15)
4	$\overline{Y16}$	O	Parallel data inverted output (inversion MSB)
5	Vdd	—	Power supply
6	CK IN	I	System clock input
7	$\overline{SCSL}$	Ip	"H" = system clock 96 fs; "L" = system clock 98 fs.
8	ABCI	Ip	44.1 kHz synchronization clock input
9	WCKI	Ip	88.2 kHz synchronization clock input
10	SIMD	Ip	"H" = serial input mode 1; "L" = serial input mode 2.
11	$\overline{BCSL}$	Ip	"H" = data readin at rise of BCKI
		Ip	"L" = data readin at fall of BCKI
12	BCKI	Ip	Bit clock input
13	DIN	Ip	Serial data input
14	Vss	—	GND
15	DGB	O	B channel de-glitch control output
16	DGA	O	A channel de-glitch control output
17	$\overline{Y1}$	O	Parallel data inverted output (inversion LSB)
18	$\overline{Y2}$	O	Parallel data inverted output (inversion BIT 2)
19	$\overline{Y3}$	O	Parallel data inverted output (inversion BIT 3)
20	$\overline{Y4}$	O	Parallel data inverted output (inversion BIT 4)
21	$\overline{Y5}$	O	Parallel data inverted output (inversion BIT 5)
22	$\overline{Y6}$	O	Parallel data inverted output (inversion BIT 6)
23	$\overline{Y7}$	O	Parallel data inverted output (inversion BIT 7)
24	$\overline{Y8}$	O	Parallel data inverted output (inversion BIT 8)
25	$\overline{Y9}$	O	Parallel data inverted output (inversion BIT 9)
26	$\overline{Y10}$	O	Parallel data inverted output (inversion BIT 10)
27	$\overline{Y11}$	O	Parallel data inverted output (inversion BIT 11)
28	$\overline{Y12}$	O	Parallel data inverted output (inversion BIT 12)