

## ■ GENERAL DESCRIPTION

The SM5804 Series is manufactured using MOLYGATE (モリゲート®) CMOS technology developed by NPC and is implemented in 4 times oversampling digital filter technique with high stopband attenuation and low passband ripple for CD player applications. This device contains digital filters for two channels and the 4 times oversampling output can be obtained from each channel so that the last stage lowpass filter can be simplified. The input and output data can be externally selected to be either serial or parallel which reduces system design restrictions. The SM5804 series has four types, Type A through Type D, classified by the filter characteristics and input data timing.

## ■ FEATURES

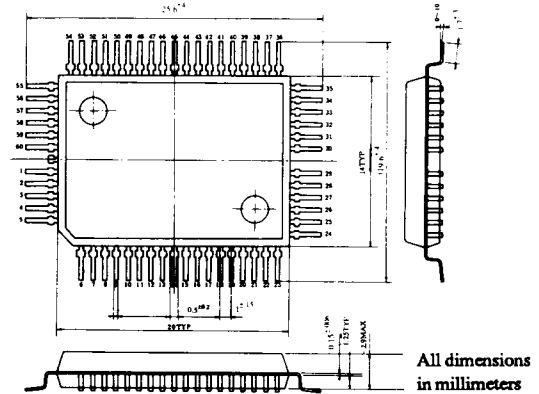
- Filter Structure
  - Dual channel filters
  - 4 times oversampling
  - Two cascaded linear phase FIR filters (80taps + 15taps)
  - 18-bit filter coefficients and 25-bit accumulator (less round-off error)
  - 16 X 18-bit multiplier
  - Overflow limiter

### • Filter Characteristics

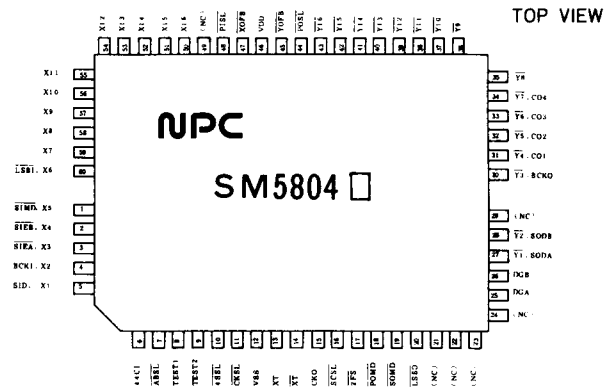
		Type A	Type B, C, and D
Passband ripple (0 ~ 20KHz)		≤ ±0.09dB	≤ ±0.015dB
Stopband attenuation	24.1 ~ 64.1KHz	≥ 90dB	≥ 70dB
	64.1KHz ~	≥ 70dB	≥ 70dB

- Compensated 3rd order Bessel filter (for type C only)
- D/A converter aperture time error correction
- Linear phase
- Input/Output
  - 16-bit serial or parallel input and output modes
  - MSB first-in/out or LSB first-in/out modes
  - 2's complement or offset binary input and output format
- Power Supply 5V ±10%
- TTL Compatible (Input and Output)
- 60-Pin Flat Package
- MOLYGATE CMOS Technology

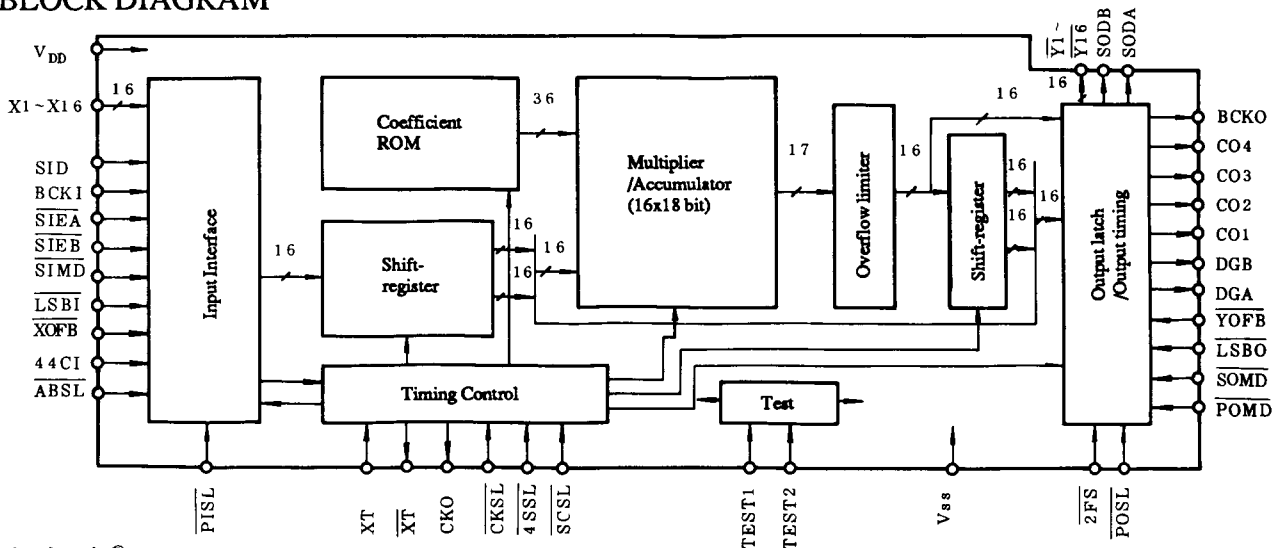
## ■ PACKAGE DIMENSIONS



## ■ PIN CONFIGURATION



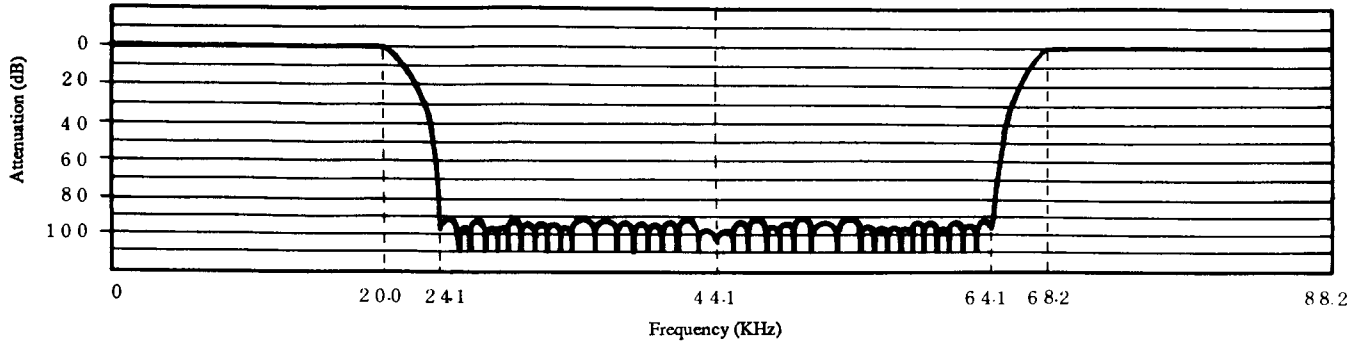
## ■ BLOCK DIAGRAM



\* モリゲート® is a registered trademark of NIPPON PRECISION CIRCUIT LTD.

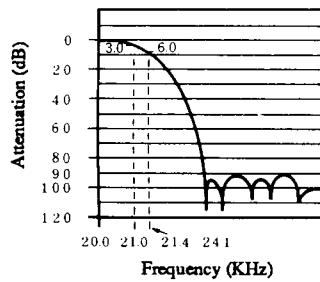
## THEORETICAL FILTER CHARACTERISTICS

• Type A

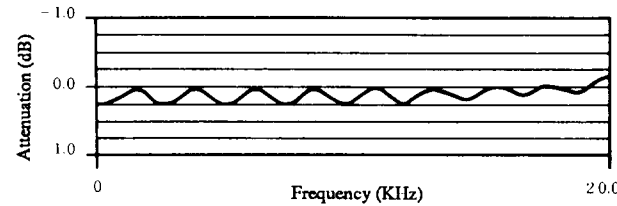


Passband	0 ~ 20KHz
Stopband	> 24.1KHz
Passband ripple	< ±0.09dB
Stopband attenuation	> 90dB

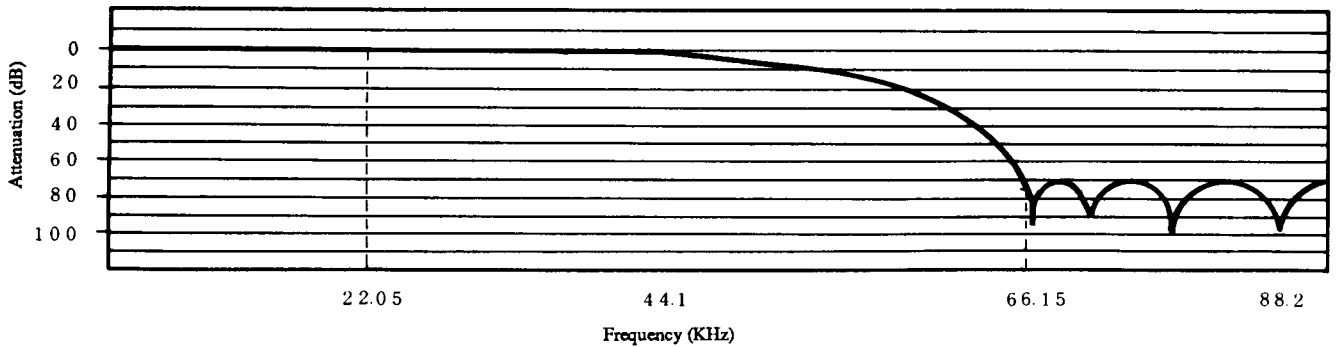
Performance Characteristic Table (1st stage)  
(f = 0 ~ 44.1KHz)



Transition Band Characteristics (1st stage)



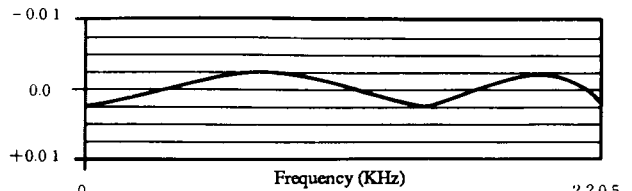
Passband Characteristics (1st stage)  
(with aperture effect correction)



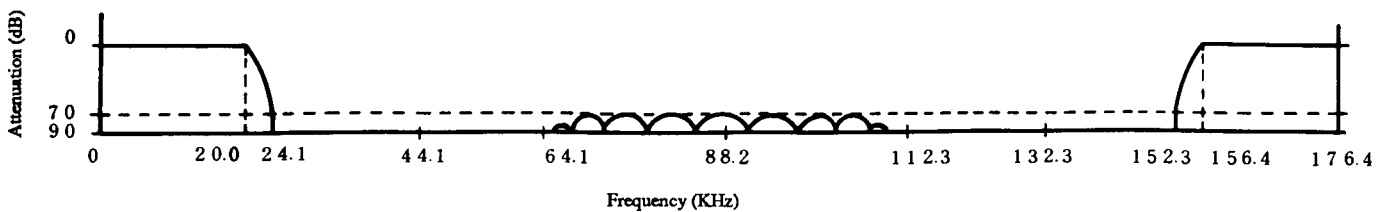
Frequency Response (2nd stage)

Passband	0 ~ 22.05KHz
Stopband	> 66.15KHz
Passband ripple	< ±0.01dB
Stopband attenuation	> 70dB

Performance Characteristic Table. (2nd stage)  
(f = 0 ~ 88.2KHz)



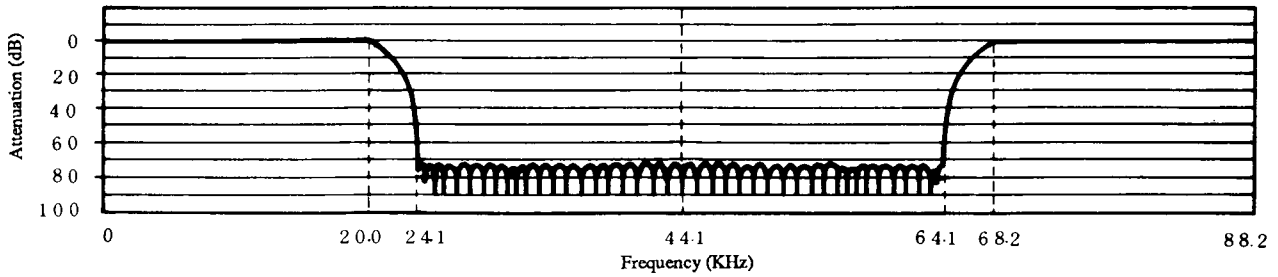
Passband Characteristics (2nd stage)  
Freq. (kHz)



Overall Frequency Response (1st and 2nd stages)

## THEORETICAL FILTER CHARACTERISTICS

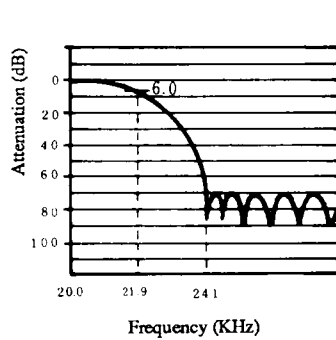
• Type B



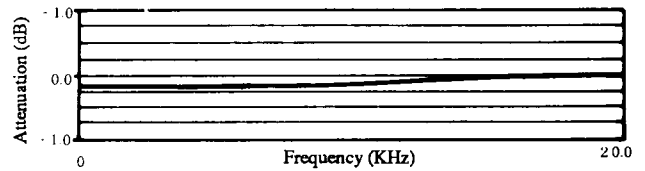
Filter Response (2nd stage)

Passband	0 ~ 20KHz
Stopband	> 24.1KHz
Passband ripple	< $\pm 0.01$ dB
Stopband attenuation	> 70dB

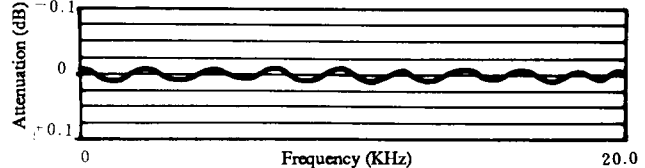
Performance Characteristic Table (1st stage)  
(f = 0 ~ 44.1KHz)



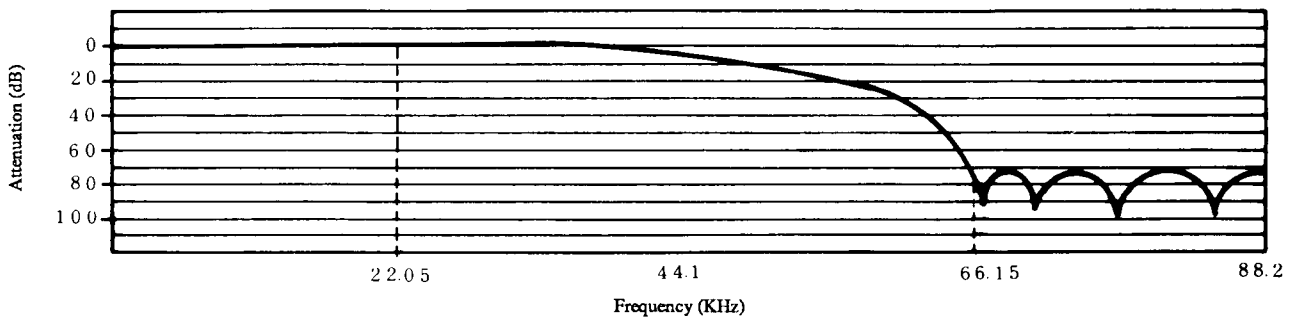
Transition Band Characteristics (1st stage)



Passband Characteristics (1st stage)  
(with aperture effect correction)



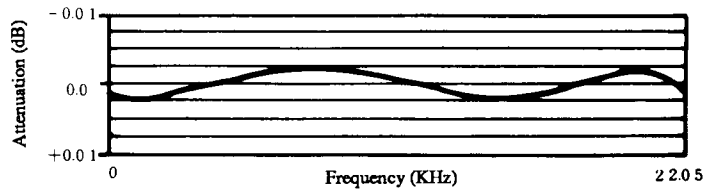
Passband Ripple Characteristics (1st stage)



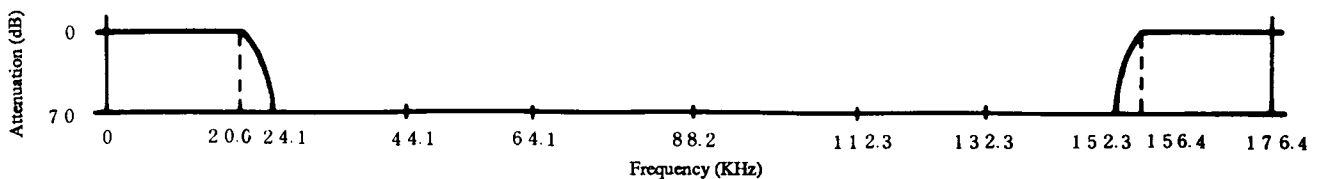
Filter Response (2nd stage)

Passband	0 ~ 22.05KHz
Stopband	> 66.15KHz
Passband ripple	< $\pm 0.005$ dB
Stopband attenuation	> 70dB

Performance Characteristic Table (2nd stage)  
(f = 0 ~ 88.2KHz)



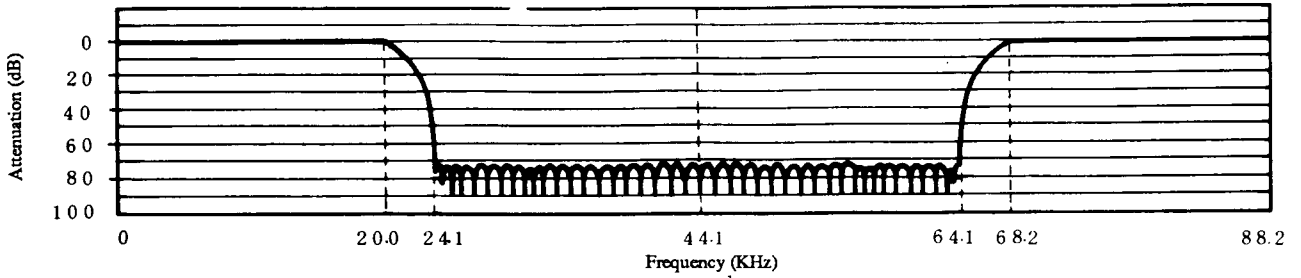
Passband Characteristics (2nd stage)



Overall Frequency Response (1st and 2nd stages)

## THEORETICAL FILTER CHARACTERISTICS

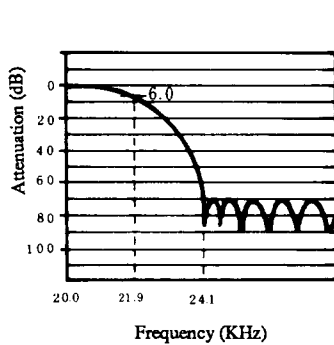
• Type C



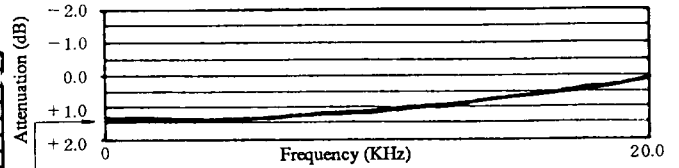
Frequency Response (1st stage)

Passband	0 ~ 20KHz
Stopband	> 24.1KHz
Passband ripple	< ±0.01dB
Stopband attenuation	> 70dB

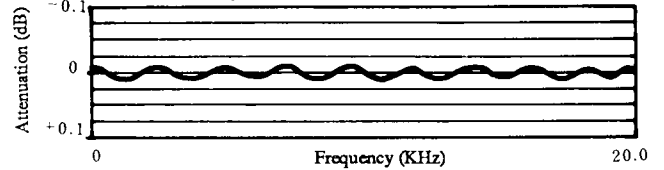
Performance Characteristic Table (1st stage)  
(f = 0 ~ 44.1KHz)



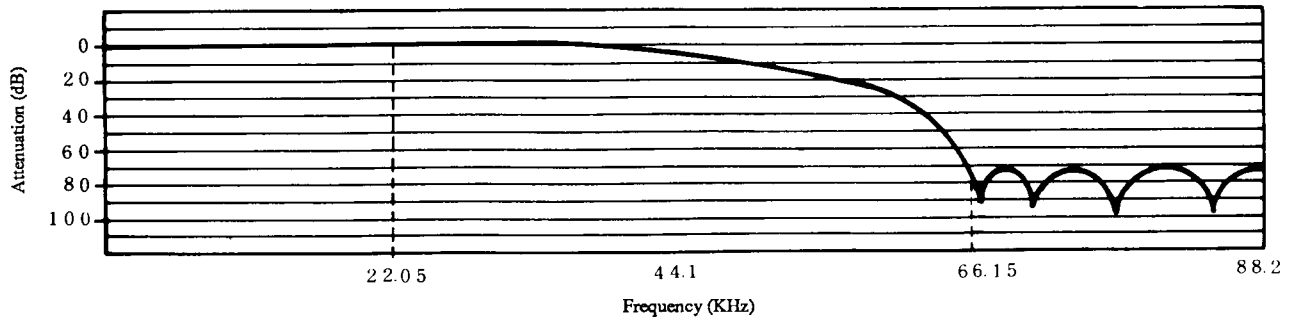
Transition Band Characteristics (1st stage)



Passband Characteristics (1st stage)  
(with aperture effect correction)



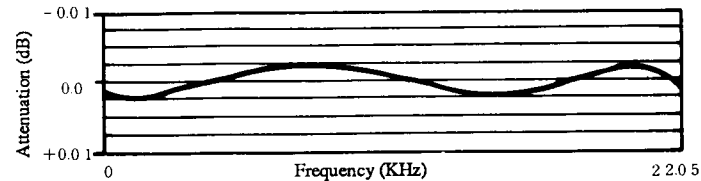
Passband Ripple Characteristics (1st stage)



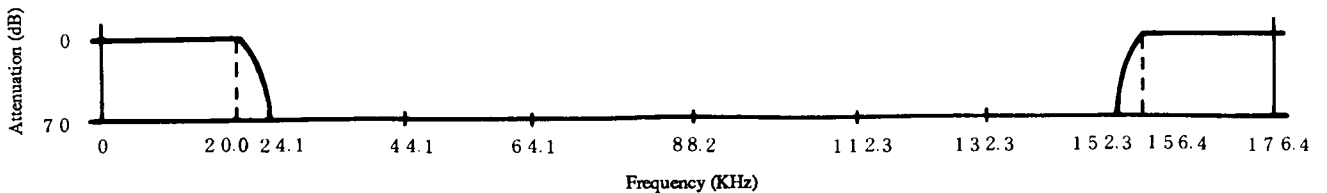
Frequency Response (2nd stage)

Passband	0 ~ 22.05KHz
Stopband	> 66.15KHz
Passband ripple	< ±0.005dB
Stopband attenuation	> 70dB

Performance Characteristic Table (2nd stage)  
(f = 0 ~ 88.2KHz)



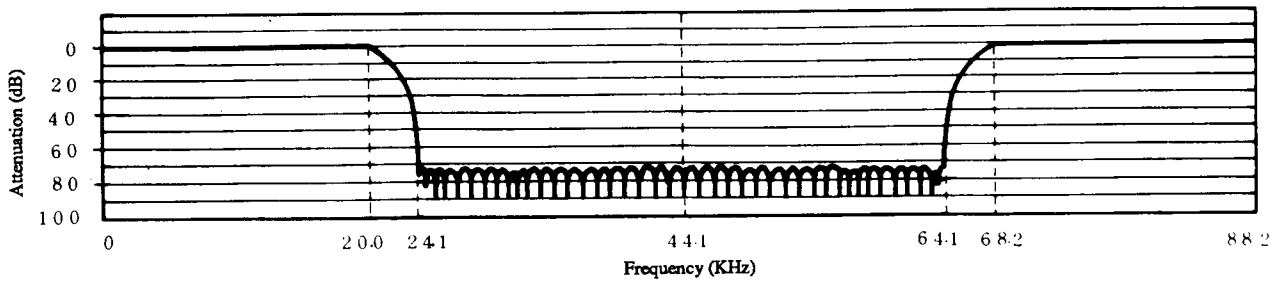
Passband Characteristics (2nd stage)



Overall Frequency Response (1st and 2nd stages)

## THEORETICAL FILTER CHARACTERISTICS

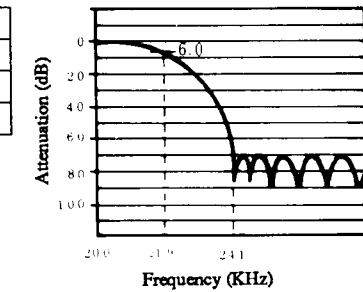
• Type D



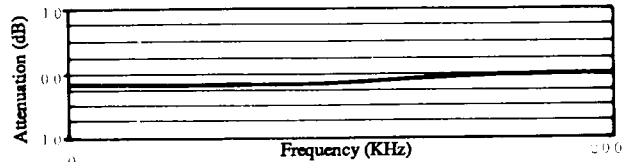
Frequency Response (1st stage)

Passband	0 ~ 20KHz
Stopband	> 24.1KHz
Passband ripple	< ±0.01 dB
Stopband attenuation	> 70dB

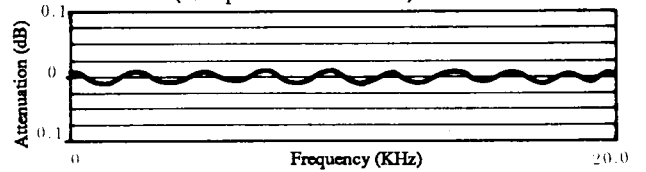
Performance Characteristic Table (1st stage)  
(f = 0 ~ 44.1KHz)



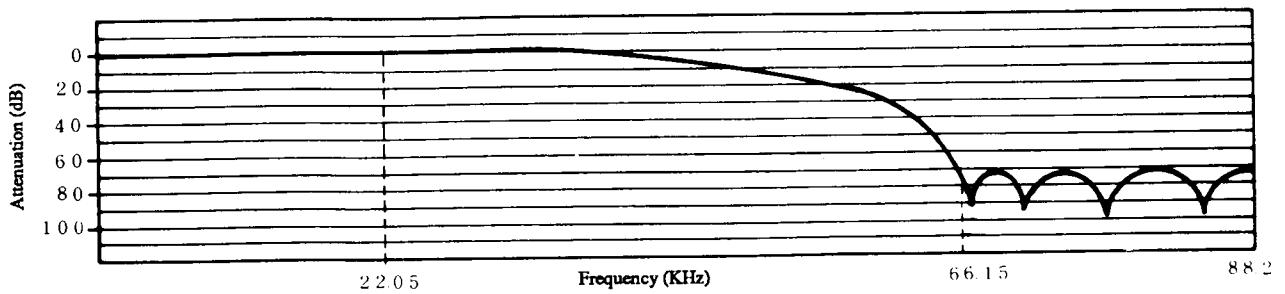
Transition Band Characteristics (1st stage)



Passband Characteristics (1st stage)  
(with aperture effect correction)



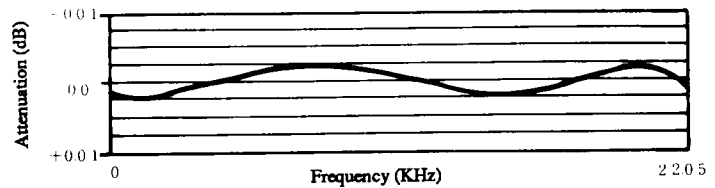
Passband Ripple Characteristics (1st stage)



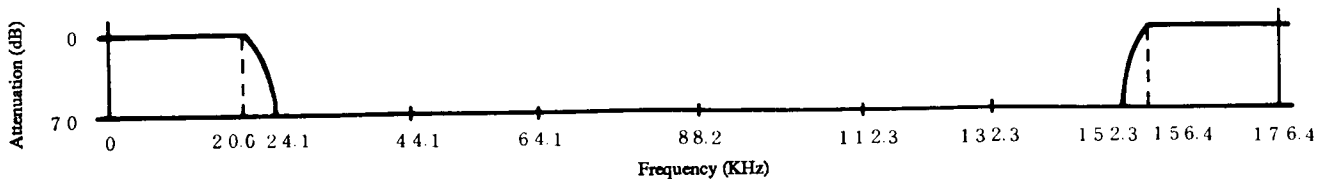
Frequency Response (2nd stage)

Passband	0 ~ 22.05KHz
Stopband	> 66.15KHz
Passband ripple	< ±0.005dB
Stopband attenuation	> 70dB

Performance Characteristic Table (2nd stage)  
(f = 0 ~ 88.2KHz)



Passband Characteristics (2nd Stage)



Overall Frequency Response (1st and 2nd stages)

■ PIN DESCRIPTION Serial Input:  $\overline{PISL} = H$ , Parallel Input:  $\overline{PISL} = L$ , Serial Output:  $\overline{POSL} = H$ , Parallel Output:  $\overline{POSL} = L$

PIN NO.	PIN NAME		FUNCTION	PIN NO.	PIN NAME		FUNCTION
	IN SERIAL	IN PARALLEL			IN SERIAL	IN PARALLEL	
1	$\overline{SIMD}$		Serial input mode select	31	CO1		Serial output control clock 1
		X5	Parallel data input (BIT5)			Y4	
2	$\overline{SIEB}$		Bch serial input enable	32	CO2		Serial output control clock 2
		X4	Parallel data input (BIT4)			Y5	
3	$\overline{SIEA}$		Ach serial input enable	33	CO3		Serial output control clock 3
		X3	Parallel data input (BIT3)			Y6	
4	BCKI		Serial bit clock input	34	CO4		Serial output control clock 4
		X2	Parallel data input (BIT2)			Y7	
5	SID		Serial data input	35	NC		
		X1	Parallel data input (LSB)			Y8	
6	44CI	←	44.1 KHz synchronization clock input	36	NC		
						Y9	
7	$\overline{ABSL}$	←	$\overline{ABSL} = H \dots 44CI H/L = Ach/Bch$ $\overline{ABSL} = L \dots 44CI H/L = Bch/Ach$	37	NC		
						Y10	
8	TEST1	←	Test pin for manufacturer use only (normally open)	38	NC		
						Y11	
9	TEST2	←	"	39	NC		
						Y12	
10	$\overline{4SSL}$	←	Normally open (see page 11 for details)	40	NC		
						Y13	
11	$\overline{CKSL}$	←	$\overline{CKSL} = H \dots$ external clock $\overline{CKSL} = L \dots$ external OSC.	41	NC		
						Y14	
12	Vss	←	GND pin	42	NC		
						Y15	
13	XT	←	$\overline{CKSL} = H \dots$ clock input $\overline{CKSL} = L \dots$ external OSC input	43	NC		
						Y16	
14	$\overline{XT}$	←	$\overline{CKSL} = H \dots$ open $\overline{CKSL} = L \dots$ external OSC input	44	$\overline{POSL}$	←	$\overline{YOFB} = H \dots$ serial output mode $\overline{YOFB} = L \dots$ parallel output mode
							←
15	CKO	←	Clock output	45	$\overline{YOFB}$	←	
							←
16	$\overline{SCSL}$	←	System clock 96fs ... $\overline{SCSL} = H$ System clock 98fs ... $\overline{SCSL} = L$	46	VDD	←	Power supply (+5V)
							←
17	$\overline{2FS}$	←	Open	47	$\overline{XOFB}$	←	$\overline{XOFB} = H \dots 2$ 's complement input data $\overline{XOFB} = L \dots$ Offset binary input data
							←
18	$\overline{POMD}$	←	$\overline{POMD} = H \dots$ Normal parallel output mode $\overline{POMD} = L \dots$ Simultaneous parallel output mode	48	$\overline{PISL}$	←	$\overline{PISL} = H \dots$ Serial input mode $\overline{PISL} = L \dots$ Parallel input mode
							←
19	$\overline{SOMD}$	←	$\overline{SOMD} = L \dots$ Serial output mode	49	NC	←	
							←
20	$\overline{LSBO}$	←	$\overline{LSBO} = H \dots$ MSB first serial output $\overline{LSBO} = L \dots$ LSB first serial output	50	NC		
						X16	
21	NC	←		51	NC		
						X15	
22	NC	←		52	NC		
						X14	
23	NC	←		53	NC		
						X13	
24	NC	←		54	NC		
						X12	
25	DGA	←	Ach deglitch control output	55	NC		
						X11	
26	DGB	←	Bch deglitch control output	56	NC		
						X10	
27	SODA		Ach serial data output	57	NC		
		Y1	Parallel data output (LSB)			X9	
28	SODB		Bch serial data output	58	NC		
		Y2	Parallel data output (BIT2)			X8	
29	NC	←	Connected to VDD internally open externally	59	NC		
						X7	
30	BCKO		Serial bit clock output	60	$\overline{LSBI}$		$\overline{LSBI} = H \dots$ MSB first serial input $\overline{LSBI} = L \dots$ LSB first serial input
		Y3	Parallel data output (BIT3)			X6	

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>DD</sub>	-0.3 ~ 7.0	V
Input Voltage	V <sub>IN</sub>	0.3 ~ V <sub>DD</sub> + 0.3	V
Storage Temp.	T <sub>STG</sub>	-40 ~ +125	°C
Power Dissipation	P <sub>w</sub>	250	mW
Soldering Temp.	T <sub>SLD</sub>	255	°C
Soldering Time	t <sub>SLD</sub>	10	Sec

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Unit
Supply Voltage	V <sub>DD</sub>	4.5 ~ 5.5	V
Oper. Temp. Range	T <sub>OPR</sub>	-20 ~ +70	°C

## ■ DC ELECTRICAL CHARACTERISTICS at Ta = -20°C ~ +70°C, V<sub>DD</sub>=4.5 ~ 5.5V, V<sub>SS</sub>=0V, unless otherwise noted

Parameter	Pin	Symbol	Condition	MAX	TYP	MAX	Unit
Supply Current	V <sub>DD</sub>	I <sub>DD</sub>	V <sub>DD</sub> =5V		30	45	mA
Input Voltage (1)	XT	V <sub>IH1</sub>		0.7V <sub>DD</sub>			V
		V <sub>IL1</sub>				0.3V <sub>DD</sub>	V
Input Voltage (2)	* 1	V <sub>IH2</sub>		2.4			V
		V <sub>IL2</sub>				0.5	V
Output Voltage	* 2	V <sub>OH</sub>	I <sub>OH</sub> = 0.4mA	2.5			V
		V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA			0.4	V
Input Leak Current	* 3	I <sub>IL</sub>	V <sub>IN</sub> = 0V			0.1	μA
	* 4	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>			0.1	μA
Input Current	* 1	I <sub>IL</sub>	V <sub>IN</sub> = 0V		10	20	μA

\*1 X1 ~ X16, 44CI, XOFB, ABSL, PISL, TEST1, TEST2, CKSL, POSL, POMD, SOMD, SCSL, LSBO, YOFB, 2FS, 4SSL

\*2 CKO, DGA, DGB, Y1 ~ Y16

\*3 XTat CKSL = H

\*4 X1 ~ X16, 44CI, XOFB, ABSL, PISL, TEST1, TEST2, CKSL, 2FS, POSL, POMD, SOMD, SCSL, LSBO, YOFB, 4SSL, XTat CKSL = H

## ■ AC ELECTRICAL CHARACTERISTICS

(1) XT Pin at Ta = -20°C ~ +70°C, V<sub>DD</sub>=4.5 ~ 5.5V, V<sub>SS</sub>=0V

a. Crystal Oscillator or External Clock  
(CKSL=L, 4SSL=L)

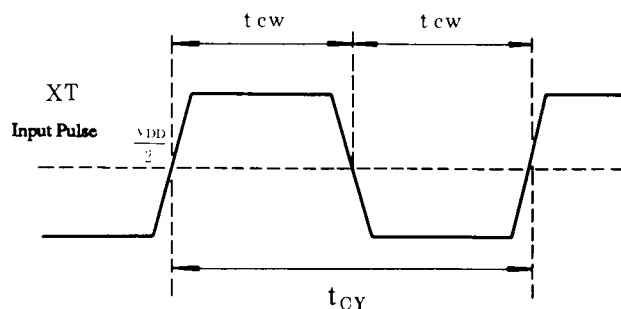
Parameter	Symbol	MIN	TYP	MAX	Unit
OSC frequency	f <sub>osc</sub>			18	MHz

b. Crystal Oscillator or External Clock  
(CKSL=L, 4SSL=H or open, or CKSL=H or open, 4SSL=L)

Parameter	Symbol	MIN	TYP	MAX	Unit
OSC frequency	f <sub>osc</sub>			9	MHz

c. External Clock  
(CKSL=H or open, 4SSL=H or open)

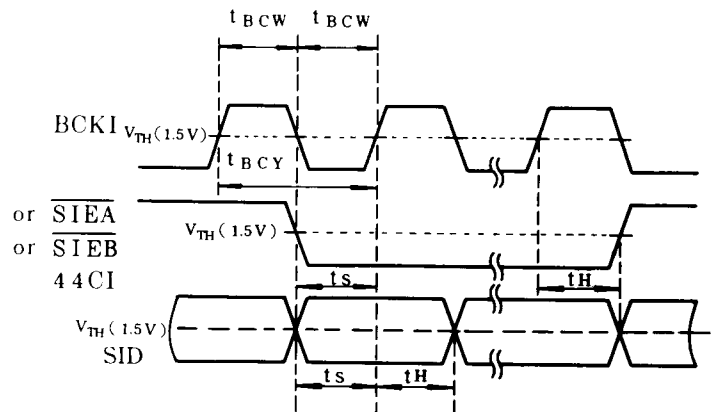
Parameter	Symbol	MIN	TYP	MAX	Unit
Clock pulse width	t <sub>cw</sub>	110			ns
Clock pulse period	t <sub>cy</sub>	220			ns



(2) Serial Input Timing ( $\overline{SID}$ , BCKI,  $\overline{SIEA}$ ,  $\overline{SIEB}$ , 44CI)

Parameter	Symbol	MIN	TYP	MAX	Unit	Comment
BCKI pulse width	t <sub>bcw</sub>	100			ns	
BCKI pulse period	t <sub>bcy</sub>	200			ns	
$\overline{SID}$ , $\overline{SIEA}$ , $\overline{SIEB}$ , 44CI setup time	t <sub>s</sub>	75			ns	note
$\overline{SID}$ , $\overline{SIEA}$ , $\overline{SIEB}$ , 44CI hold time	t <sub>h</sub>	75			ns	

Note: For  $\overline{SIEA}$ ,  $\overline{SIEB}$ ,  $\overline{SIMD}$  = H or open  
For 44CI,  $\overline{SIMD}$  = L



Timing waveforms when  $\overline{SIMD}$  = H or open

## INTRODUCTION

### Basic Filter Structure

The SM5804 series consists of two channel filters implemented in two times oversampling two stages cascaded linear phase FIR filter as shown in Fig. 1. The 44.1KHz sampled signal is two times oversampled in the 80-tap first filter stage and is converted to a 88.2KHz sampled signal. It is further two times oversampled in the 15-tap second filter stage and becomes 176.4KHz sampled signal which is 4 times oversampled as compared with that at the input.

Fig. 2 illustrates sampled signal spectrum of the output of channel filter (see Fig. 1) in various configurations. Fig. 2(a) shows the output spectra of the first filter which provides -90dB or -70dB attenuation at and above 24.1KHz in Type A or Type B, C and D configuration respectively. However, the input signal spectrum of  $\pm 24.1$ KHz centered on 88.2KHz sampling frequency still exists. The second filter which further doubles the sampling frequency for filtering the output of the first filter provides -70dB attenuation for the signal band between 64.1KHz and 112.3KHz as shown in Fig. 2(b). The combined filter characteristics of Type A and Type B, C and D are illustrated in Fig. 2(c) and (d) respectively. A simple 3rd order active lowpass filter may be used as a postfilter following the SM5804 second filter stage. The SM5804 series are designed based on this oversampling technique and their filter characteristics are illustrated in page 2 through 5.

### Block Diagram

Fig. 3 is SM5804 series filter block diagram. Two channel filters, Ach and Bch operate independently and their inputs and outputs can also be independently selected to operate in serial or parallel mode.

### Application Examples

As the input and output can be independently selected for serial/parallel mode, the external DAC which follows the SM5804 can also be connected in various ways. Six examples are illustrated in Fig. 4.

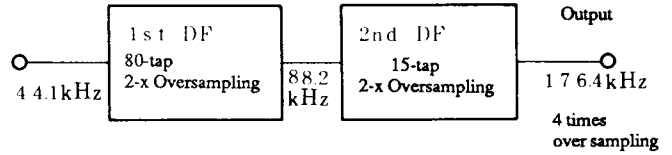


Figure 1 Block Diagram of the Channel Filter

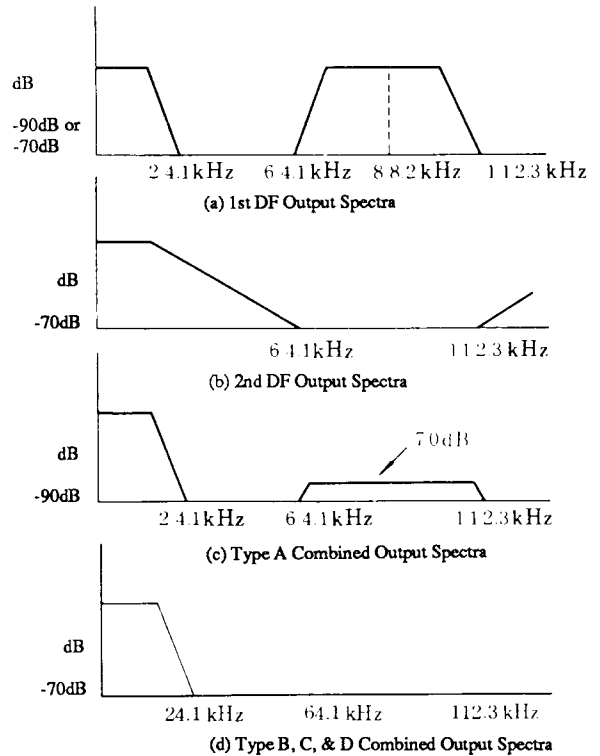


Figure 2 Signal Spectra

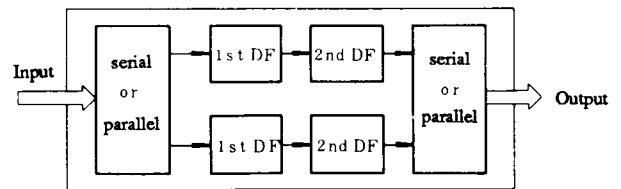


Figure 3 Block Diagram of MS5804

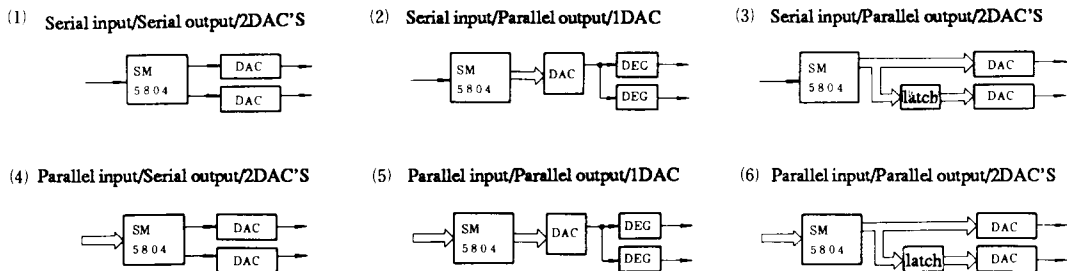


Figure 4 Applications



## FUNCTIONAL DESCRIPTION

### (1) Serial/Parallel mode select

Input and output data can be independently selected to either serial mode or parallel mode through  $\overline{\text{PISL}}$  and  $\overline{\text{POSL}}$  respectively.

Input:	$\overline{\text{PISL}} = \text{H}$ (or open)	Serial Input
	$\overline{\text{PISL}} = \text{L}$	Parallel Input
Output:	$\overline{\text{POSL}} = \text{H}$ (or open)	Serial Output
	$\overline{\text{POSL}} = \text{L}$	Parallel Output

### (2) 2's Complement/Offset binary code select

Input and output data format can be independently selected to either 2's complement or offset binary through  $\overline{\text{XOFB}}$  and  $\overline{\text{YOFB}}$ .

Input:	$\overline{\text{XOFB}} = \text{H}$ (or open)	2's complement
	$\overline{\text{XOFB}} = \text{L}$	offset binary
Output:	$\overline{\text{YOFB}} = \text{H}$ (or open)	2's complement
	$\overline{\text{YOFB}} = \text{L}$	offset binary

### (3) Ach and Bch Data synchronization

One frame of the input sampled data (consisting of Ach and Bch data) is processed simultaneously. Therefore, synchronization of the Ach and Bch input data pair is necessary to avoid phase difference between two channels due to the different sampling time slot. Pin  $\overline{\text{ABSL}}$  is provided to synchronize Ach and Bch data to either rising or falling edge of the synchronization clock (44CI, 44.1KHz) to prevent channel phase difference. However, if  $\overline{\text{SIEA}}$  and  $\overline{\text{SIEB}}$  are used for serial input mode,  $\overline{\text{ABSL}}$  pin can be ignored.

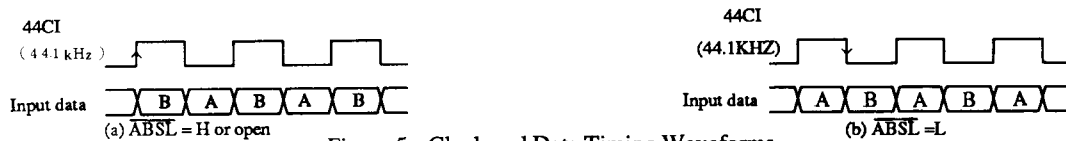


Figure 5 Clock and Data Timing Waveforms

### (4) Phase Relation between 44CI and XT clocks

The system clock XT must stay "high" for 30ns before and 5ns after the rising transition (when  $\overline{\text{ABSL}}=\text{H}$ ) or the falling transition (when  $\overline{\text{ABSL}}=\text{L}$ ) of the synchronization clock 44CI. i.e. The shaded area of the Fig. 6 must fall within the "high" cycle of clock XT.

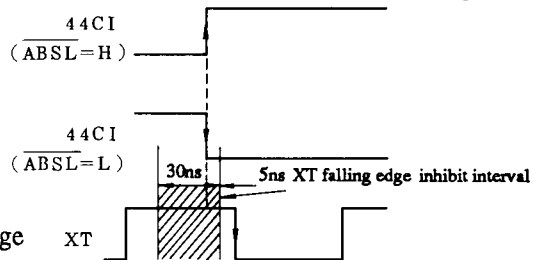


Figure 6 44CI and XT Clocks Timing Waveforms

### (5) Serial input mode ( $\overline{\text{PISL}} = \text{H}$ or open)

The following steps/conditions apply to serial input mode operation.

- (i) Connect input data line to Pin SID.
- (ii) Read timing is selected by applying "H" or "L" voltage level to Pin  $\overline{\text{SIMD}}$ .

- When  $\overline{\text{SIMD}} = \text{H}$  or open

In this mode, serial input bit clock, BCKI, and Ach and Bch serial input enables  $\overline{\text{SIEA}}$  and  $\overline{\text{SIEB}}$  are involved. The data is clocked into the shift register at the rising edge of BCKI while  $\overline{\text{SIEA}}$  and  $\overline{\text{SIEB}}$  are at "L". It is therefore required that changing of data state must take place at the falling edge of BCKI. Data will be transferred and latched in parallel into other registers at the falling edge of  $\overline{\text{SIEA}}$  or  $\overline{\text{SIEB}}$  after the 16-bit data has been read.

- When  $\overline{\text{SIMD}} = \text{L}$

In this mode, serial input bit clock, BCKI, and 44CI clock are involved. The data is clocked into the shift register at the rising edge of BCKI and the change of data state is allowed at falling edge of BCKI. Data will be transferred and latched in parallel by the 44CI clock at either rising or falling edge of the clock.

#### (iii) MSB first-in/LSB first-in select

MSB first-in or LSB first-in is selected by using the  $\overline{\text{LSBI}}$  pin as follows:

$\overline{\text{LSBI}} = \text{H}$ or open,	MSB first-in
$\overline{\text{LSBI}} = \text{L}$ ,	LSB first-in

NOTE: In serial input mode, X7 through X16 pins are not used. However, any interference to these pins does not effect performance and accuracy of the device.

(6) Parallel input mode ( $\overline{\text{PISL}} = \text{L}$ )

The following steps/conditions apply to parallel input mode operation.

- (i) Connect input data lines to Pin X1 through X16 (X1 = LSB, X16 = MSB).
- (ii) Connect 44.1KHz (50% duty cycle) synchronization clock to Pin 44CI.

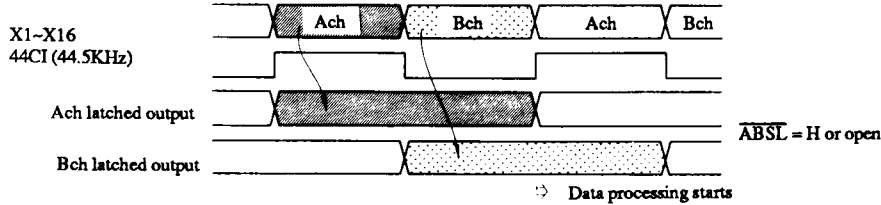


Figure 7 Input, Output and Clock Timing Waveforms.

(iii) Read timing

Ach and Bch parallel data are read at the second falling edge of the system clock, XT (approx. 4MHz) after the transition of the synchronization clock, 44CI. See Fig. 8.

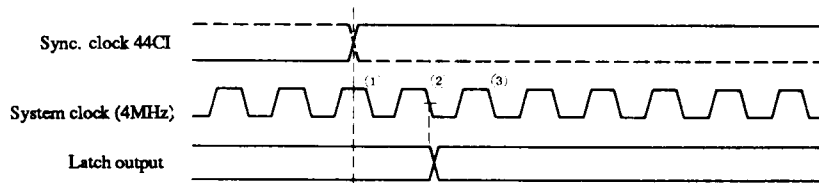


Figure 8 Sync clock, System Clock and Output Timing Waveforms.

(7) Data processing starting timing

When the input data is in parallel or serial mode with  $\overline{\text{SIMD}} = \text{L}$ , the data processing starts at the rising edge of 44CI for  $\overline{\text{ABS}}\text{L} = \text{H}$  or open, or the falling edge of 44CI for  $\overline{\text{ABS}}\text{L} = \text{L}$

When the input data is in serial mode with  $\overline{\text{SIMD}} = \text{H}$  or open, the data processing starts at the rising edge of  $\overline{\text{SIEB}}$ .

(8) Serial output mode ( $\overline{\text{POS}}\text{L} = \text{H}$  or open,  $\overline{\text{SOMD}} = \text{L}$ )

The following conditions apply to serial output mode operation.

(i) Serial output data for Ach and Bch are available at SODA and SODB respectively. Serial output data is synchronized to the falling edge of the output bit clock running at the same frequency of system clock.

(ii) MSB first-out/LSB first-out select

MSB first-out or LSB first-out mode can be selected by Pin  $\overline{\text{LSBO}}$ .

MSB first-out  $\overline{\text{LSBO}} = \text{H}$  or OPEN

LSB first-out  $\overline{\text{LSBO}} = \text{L}$

In the serial output mode,  $\overline{\text{Y10}} \sim \overline{\text{Y16}}$  pins are not used and stay at high impedance state.

(9) Parallel output mode ( $\overline{\text{POS}}\text{L} = \text{L}$ )

The following conditions apply to parallel output mode operation.

(i) Parallel data outputs are available at  $\overline{\text{Y1}} \sim \overline{\text{Y16}}$  pins ( $\overline{\text{Y1}} = \text{LSB}$ ,  $\overline{\text{Y16}} = \text{MSB}$ )

(ii) Pin  $\overline{\text{POMD}}$  provides the options for the number of DAC to be connected.

$\overline{\text{POMD}} = \text{H}$  or open One DAC application

$\overline{\text{POMD}} = \text{L}$  Two DAC's in phase conversion application. See Fig. 1, page 14 for circuit connection.

(10) DAC control signal

DGA, DGB as well as CO1 - CO4 are used as control signals for DAC.

The following pin combinations are defined for different selected output modes.

In serial output mode, use Pin CO1~CO4, DGA and DGB.

In parallel output mode, use Pin DGA and DGB.

Refer to the operation mode table, Table 1 on page 11 for details.

(11) Input and Output time delay

See page 11 for details.

# OPERATING MODES TABLE

- Input and Output Modes Selections

Input			Output			DAC Control Signal									
Data form	Para/Serial	Data flow	Read timing	Data processing starting point	Data form	Para/Serial	Data flow	DAC	Output Timing	CO1	CO2	CO3	CO4	DGA	DGB
$\overline{XORB} = H$ 2's complement	H	$\overline{LSBI} = H$ MSB first	$\overline{SIMD} = H$ • Read at rising edge of $\overline{BCKI}$ while $\overline{SIEH}, \overline{SIEB} = L$ .	Rising edge of $\overline{SIEB}$	$\overline{YORFB} = H$ 2's complement	H (serial)	$\overline{LSBO} = H$ MSB first	$\overline{SOMD} = L$ 2 DAC'S	45th falling edge of XT after 44CI changes state. Synchronized to $\overline{BCKO}$ 's rising edge.	44.1 KHz	88.2 KHz	176.4 KHz	88.2 KHz	DGA	DGB
$\overline{XORFB} = L$ offset binary	$\overline{PISL} =$	$\overline{LSBI} = H$ LSB first	• Latch at rising edge of $\overline{SIEA}, \overline{SIEB}$ $\overline{SIMD} = L$ • Read at rising edge of $\overline{BCKI}$	$\overline{ABSIL} = H$ is rising edge of 44CI	$\overline{YORFB} = L$ offset binary					88.2 KHz	88.2 KHz	88.2 KHz	88.2 KHz	Ach deglitch (duty 25%)	Bch deglitch (duty 25%)
	(parallel)	(parallel)	• Latch at rising or falling edge of 44CI 2nd falling edge of XT after 44CI changes state	$\overline{ABSIL} = L$ is falling edge of 44CI		L (parallel)		$\overline{POMD} = H$ 1 DAC	45th falling edge of XT after 44CI changes state.	DGA	DGA	DGA	DGA	DGA	DGB
								$\overline{POMD} = L$ 2 DAC'S		Ach output external latch clock	Ach output external latch clock	Ach output external latch clock	Ach output external latch clock	Ach output external latch clock	Ach output external latch clock

Table 1 Input and Output Modes Selection

\*1 Input and output modes can be selected independently.

\*2 "H" means connected to VDD or open.

## System Clock Selections

SM5804 Series operates with a clock frequency of 96fs=4.2336MHz or 98fs=4.3218MHz (fs is sampling frequency) and Pin 4SSL is normally at "H" or open. Pin CKSL is to select external clock or crystal oscillator to the device. However, external clock can be connected through crystal oscillator pins. In case of sharing the clock with  $\mu P$  or DAC, set Pin 4SSL, CKSL, SCSL voltage levels according to Table 2 for the correct clock frequency.

4SSL and clock origin	4SSL="H" (or Open)		4SSL="L"	
	external clock	xial OSC/external clock	external clock	xial OSC/external clock
SCSL	$\overline{CKSL} = H$	$\overline{CKSL} = L$	$\overline{CKSL} = H$	$\overline{CKSL} = L$
XT, XT clock output (CKO) system clock (internal)	4.2336MHz (96fs)	4.3218MHz (98fs)	8.4672MHz (192fs)	8.6436MHz (196fs)
	$\overline{SCSL} = H$	$\overline{SCSL} = L$	$\overline{SCSL} = H$	$\overline{SCSL} = L$
	4.2336MHz (96fs)	4.3218MHz (98fs)	8.4672MHz (192fs)	8.6436MHz (196fs)
	$\overline{CKSL} = H$	$\overline{CKSL} = L$	$\overline{CKSL} = H$	$\overline{CKSL} = L$
	4.2336MHz (96fs)	4.3218MHz (98fs)	8.4672MHz (192fs)	8.6436MHz (196fs)

Table 2 System Clock Selections

# SM5804

- Output to Input Delay Time  
There is a time delay between output data frame and input data frame due to the time required for data processing. This delay time, TOF is defined in Fig. 9.

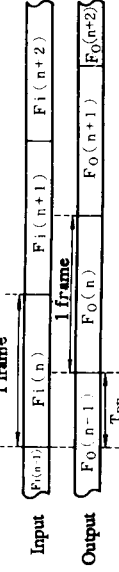


Figure 9 Input and Output Word Frames

- Synchronization of frame data

In order to process the in phase data as a frame, Pin ABSL sets Ach and Bch data pair synchronization to either rising or falling edge of 44CI as shown in Figure 10.

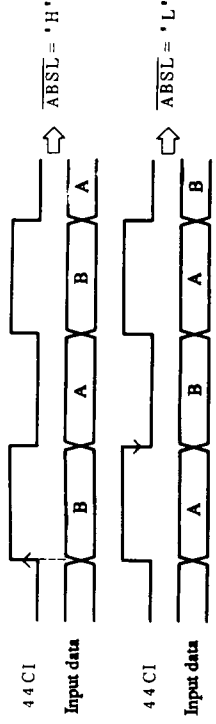
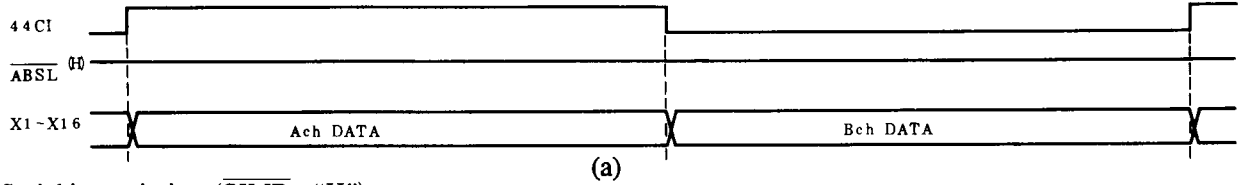


Figure 10 Input and Snyrn.Clock Timing Waveforms

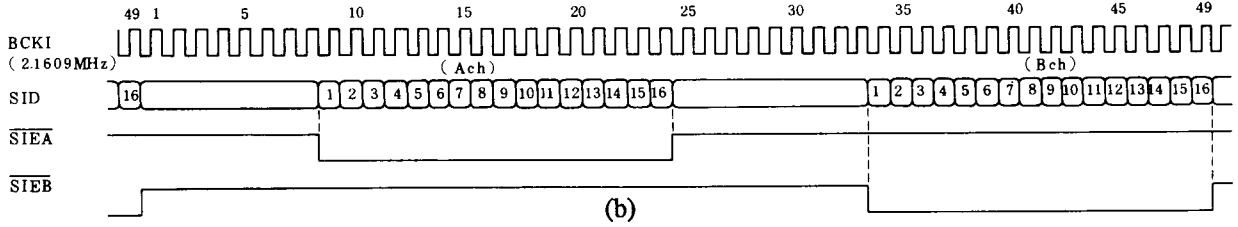
## ■ TIMING DIAGRAMS

### • Input Timing

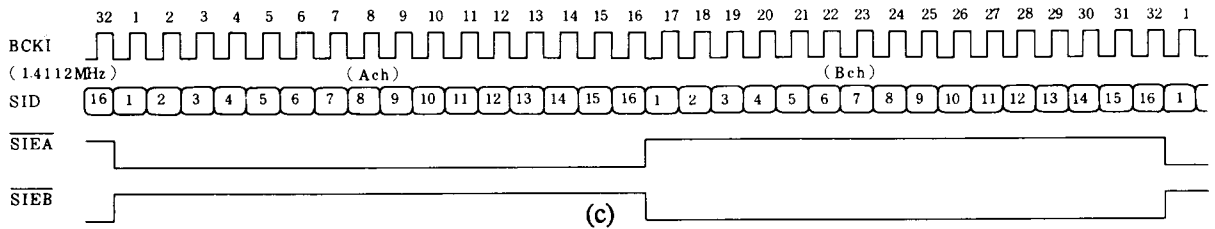
#### (1) Parallel input timing ( $\overline{ABSL} = "H"$ )



#### (2) Serial input timing ( $\overline{SIMD} = "H"$ )

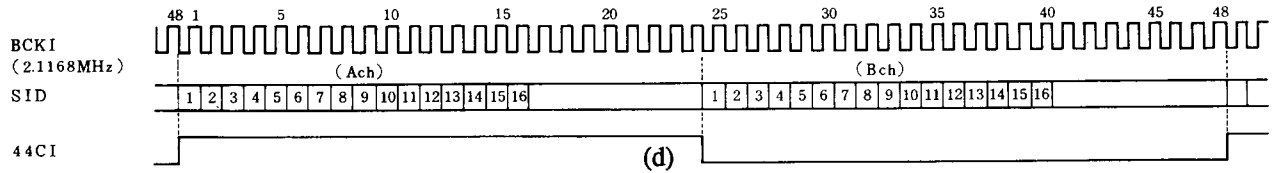


#### (3) Serial input timing ( $\overline{SIMD} = "H"$ )



#### (4) Serial input timing ( $\overline{SIMD} = "L", \overline{ABSL} = "H"$ )

##### • Type A & B



##### • Type C & D

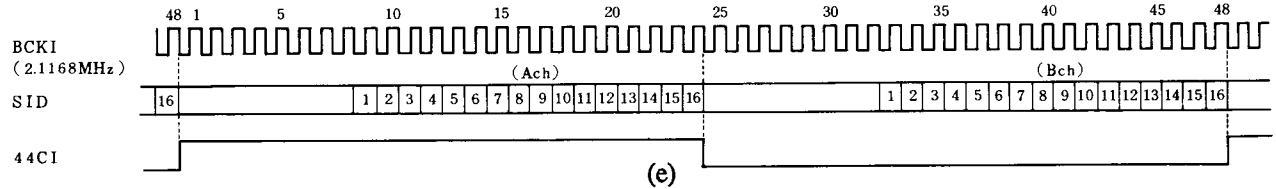
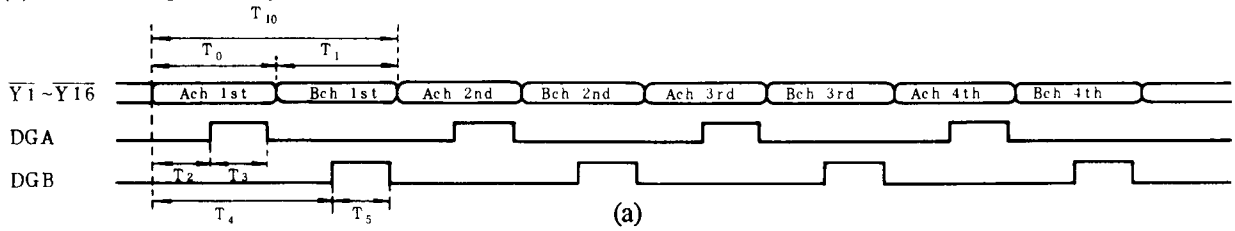


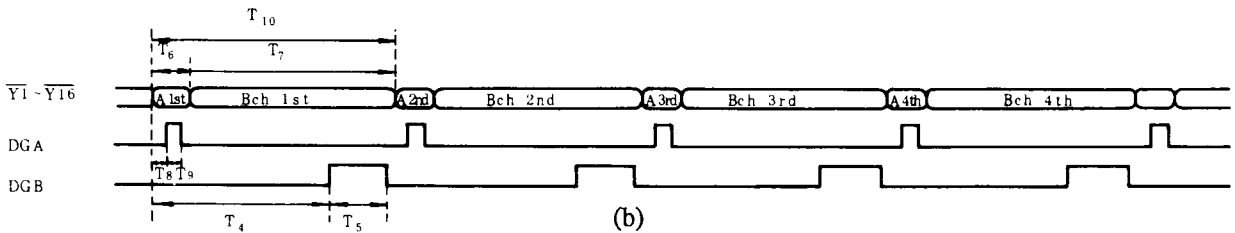
Figure 11 Input Data Timing Diagrams

• Output Timing

(5) Parallel output timing ( $\overline{\text{POMD}} = \text{"H"}\text{"}$ )



(6) Parallel output timing ( $\overline{\text{POMD}} = \text{"L"}\text{"}$ )



Time System Clock	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
96fs (4.2336MHz)	2.83	2.83	1.30	1.30	4.13	1.30	1.06	4.61	0.35	0.35	5.67
98fs (4.3218MHz)	2.89	2.78	1.39	1.27	4.16	1.30	1.16	4.51	0.46	0.35	5.67

(7) Serial output timing ( $\text{SOMD}=\text{L}, \text{SCSL}=\text{H}, \text{system clock}=4.2336\text{MHz}$ )

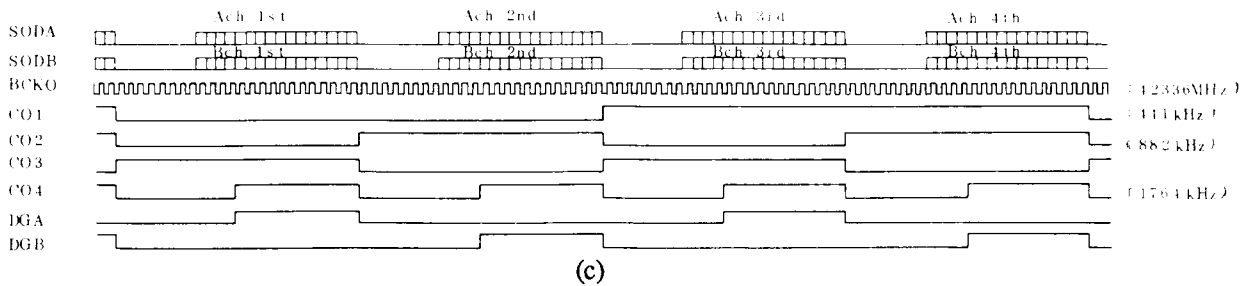
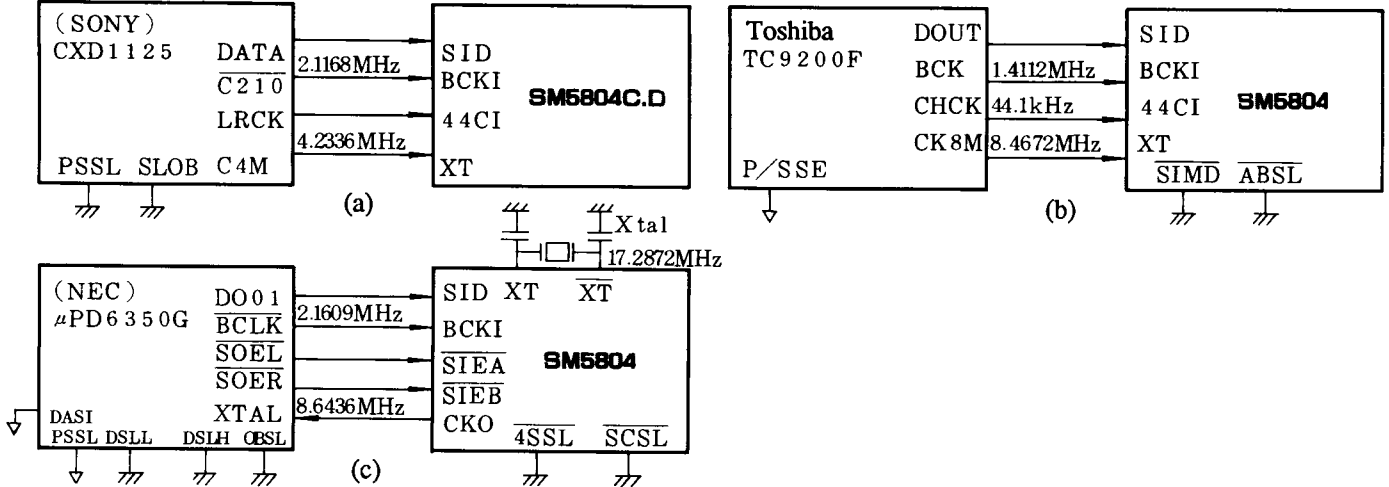


Figure 12 Output Data Timing Diagrams

## SYSTEM APPLICATION DIAGRAMS

### Input connection

#### (1) Serial input



#### (2) Parallel input

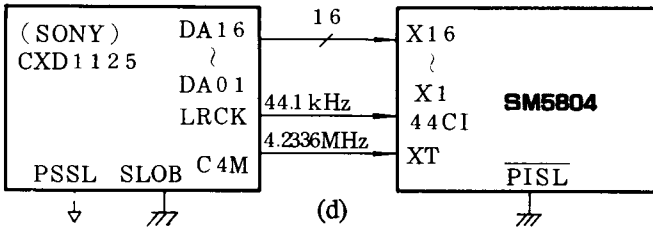
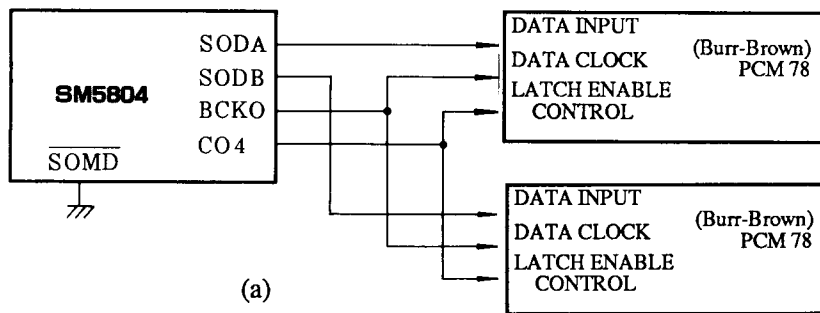


Figure 13 Application Circuits - Serial/Parallel Input Connections

### Output connection

(1) Serial output In serial output mode, system clock must be  $96fs = 4.2336 \text{ MHz}$  ( $fs = 44.1\text{KHz}$ )



#### (2) Parallel output (in-phase conversion)

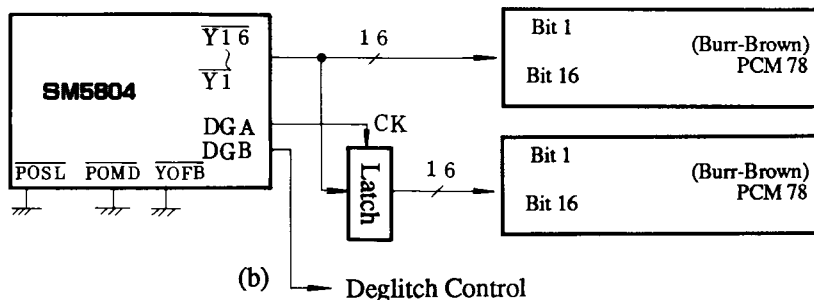


Figure 14 Application Circuits - Serial/Parallel Output Connections

All specifications are subject to change without notice.

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