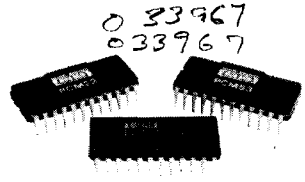
BURR-BROWN®



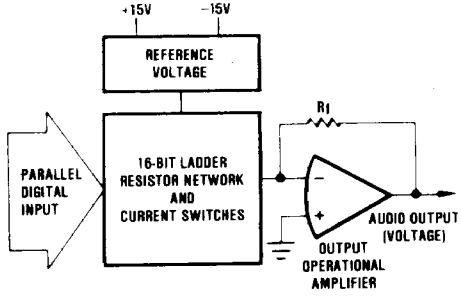
PCM52JG-V
PCM53JG-V
PCM53JP-V
PCM53JG-I

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.002% THD (FS Input, 16 Bits), typ
- 0.02% THD (-20dB, 16 Bits), typ
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V (PCM53) AND ±5V (PCM52) AUDIO OUTPUT AVAILABLE
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PIN OUT
- COMPACT, 24-PIN, DIL PACKAGE



DESCRIPTION

The PCM52 and PCM53 are state-of-the-art, fully monolithic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM52-V and PCM53-V are completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier, all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast-settling time required for critical audio applications. The converters can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliability and outstanding overall system performance.

The PCM53JG-I is similar to the PCM53JG-V except it provides a current output that settles to within ±0.006% of FSR of its final value in typically 350nsec in response to a full-scale change in the digital input code.

The letters JG and JP after the number (PCM53JG or PCM53JP) refer to the package type: the JG refers to a ceramic DIP package and JP refers to a plastic molded package. The letters -V and -I (PCM53JG-V and PCM53JG-I) refer to the voltage-output and current-output models respectively. These models are currently available: PCM52JG-V, PCM53JG-V, PCM53JP-V, PCM53JG-I. Other family members may become available later.

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SPECIFICATIONS

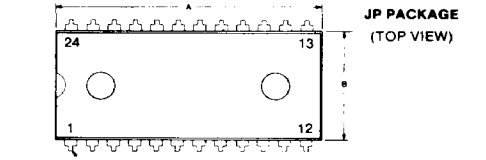
ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted.

MODEL	PCM52/PCM53			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL/CMOS Compatible): Logic "1" at +40µA	+2.4		+V_{CC}	VDC
Logic "0" at −0.5mA	0		+0.8	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±0.1	±1.0	%
Bipolar Zero Error[1]		±10	±50	mV
Differential Linearity Error at Bipolar Zero		0.001	0.005	% of FSR[2]
Noise (rms)(20Hz to 20kHz) at Bipolar Zero: PCM52-V[3]		15	30	µV
PCM53-V[3]		30	60	µV
TOTAL HARMONIC DISTORTION[4] (16-Bit Resolution)				
V_O = ±FS at f = 420Hz		0.002	0.004	%
V_O = −20dB at f = 420Hz		0.02	0.04	%
V_O = −60dB at f = 420Hz		1.9	4.0	%
MONOTONICITY		16		Bits
DRIFT (0°C to +70°C)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±150	ppm of FSR/°C
		±0.1	±0.68	% of FSR
		±0.01	±0.06	dB
Bipolar Zero Drift		±4	±20	ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Models (PCM52-V, PCM53-V) Output: 10V Step		3		µsec
1LSB Step		1		µsec
Current Model (PCM53-I) Output (1mA Step): 10Ω to 100Ω Load		350		nsec
1kΩ Load[7]		350		nsec
Deglitcher Delay (THD Test)[5]		2.5	4.0	µsec
Slew Rate		10		V/µsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges: PCM53-V	±9.8	±10	±10.2	V
PCM52-V	±4.9	±5	±5.1	V
Output Current	±5			mA
Output Impedance		0.1		Ω
Short-Circuit Duration		Indefinite to Common		
Current Model				
Range, PCM53-I (±30%)		±1		mA
Output Impedance (±30%)		2.4		kΩ
POWER SUPPLY				
SENSITIVITY				
+V_{CC}		±0.001		% of FSR/%V_{CC}
−V_{CC}		±0.001		% of FSR/%V_{CC}
V_{DD}		±0.001		% of FSR/%V_{CC}
POWER SUPPLY REQUIREMENTS				
Voltage: ±V_{CC}[6]	±14.25	±15	±15.75	VDC
V_{DD}[6]	+4.75	+5	+15.75	VDC
(V_{DD} may be connected to +V_{CC} supply voltage. Result is slightly increased total power dissipation of approximately 40mW)				
Supply Drain (no load): +V_{CC}[6]		+18	+30	mA
−V_{CC}[6]		−18	−30	mA
V_{DD}[6]		+4	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C

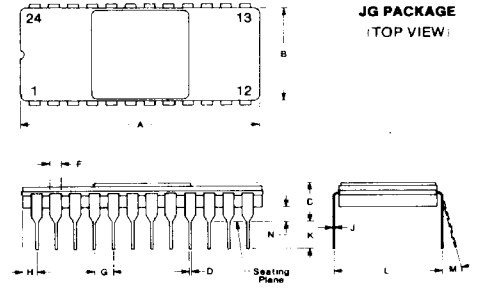
NOTES: 1. Adjustable to zero with external potentiometer. 2. FSR means Full Scale Range and is 20V for ±10V (PCM53-V) and 10V for ±5V range (PCM52-V). 3. Characterization units show at least two sigma units to meet this specification. Not 100% final tested. 4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 2. Burr-Brown may calculate THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. 5. Deglitcher or Sample/Hold delay used in THD measurement test circuit. See Figures 2 and 3. 6. See Connection Diagram and Pin Assignments. 7. Measured with an active clamp to provide a low impedance for approximately 200nsec.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.263	31.32	32.08
B	.538	.578	13.67	14.61
C	.160	.224	4.28	5.70
D	.015	.023	0.38	0.58
F	.043	.062	1.08	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.016	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE:
Leads in true position within 0.10" (0.25mm R at MMC at seating plane.



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

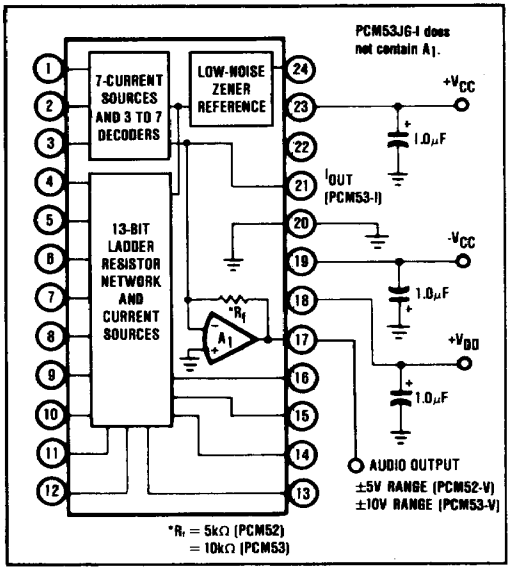
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.237	1.263	31.42	32.08
B	.514	.526	13.06	13.36
C	.178	.230	4.52	5.84
D	.016	.020	0.41	0.51
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.065	.085	1.65	2.16
J	.008	.012	0.20	0.30
K	.100	.200	2.54	5.08
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.035	.055	0.89	1.40

Actual package, such as cover appearance, may vary slightly from unit to unit. Pin spacing will not change.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	-1V to +Supply Voltage
Storage Temperature	-55°C to +100°C
Lead Temperature During Soldering	10sec at +300°C

CONNECTION DIAGRAM



PIN ASSIGNMENTS

PIN NO.	PCM52/53-V	PIN NO.	PCM53-I
1	Bit 1 (MSB)	1	Bit 1 (MSB)
2	Bit 2	2	Bit 2
3	Bit 3	3	Bit 3
4	Bit 4	4	Bit 4
5	Bit 5	5	Bit 5
6	Bit 6	6	Bit 6
7	Bit 7	7	Bit 7
8	Bit 8	8	Bit 8
9	Bit 9	9	Bit 9
10	Bit 10	10	Bit 10
11	Bit 11	11	Bit 11
12	Bit 12	12	Bit 12
13	Bit 13	13	Bit 13
14	Bit 14	14	Bit 14
15	Bit 15	15	Bit 15
16	Bit 16 (LSB)	16	Bit 16 (LSB)
17	±5V AUDIO OUT (PCM52-V) ±10V AUDIO OUT (PCM53-V)	17	R_f (10kΩ ±30%)
18	V_{DD}	18	V_{DD}
19	$-V_{CC}$	19	$-V_{CC}$
20	COMMON	20	COMMON
21	SUMMING JUNCTION	21	I_{OUT}, ±1mA ±30% (AUDIO OUTPUT)
22	TEST POINT	22	TEST POINT
23	$+V_{CC}$	23	$+V_{CC}$
24	REFERENCE OUT (+6.3V)	24	REFERENCE OUT (+6.3V)

THEORY OF OPERATION AND AUDIO SPECIFICATIONS

The transfer function of an ideal binary D/A converter is a set of discrete output levels that lie on a straight line as shown in Figure 1. The number of possible discrete output levels, or resolution, is equal to 2^n where n is the number of digital inputs or "bits". The PCM52/53 has 2^{16} or 65,536 possible output levels. Another method of expressing resolution that is useful in audio applications is Dynamic Range.

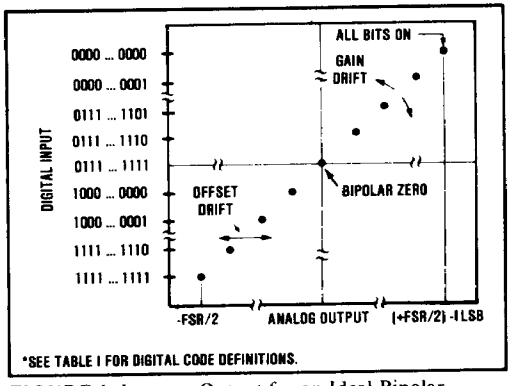


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error in unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM52/53 is shown in Figure 2. A timing diagram for the control logic is shown in Figure 3.

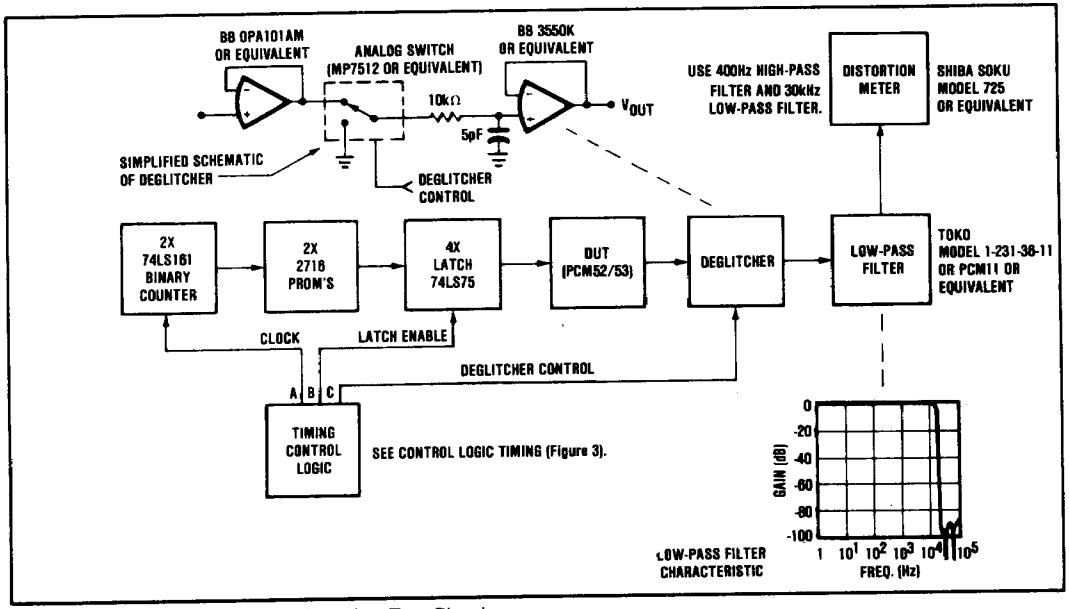


FIGURE 2. Block Diagram of Distortion Test Circuit.

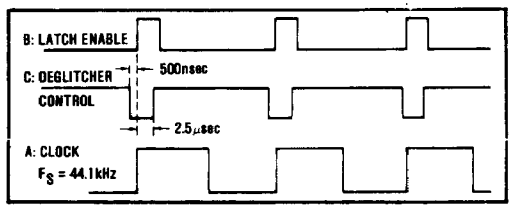


FIGURE 3. Control Logic Timing for PCM52/53 Distortion Test Circuit.

If we assume that the error due to the test circuit is negligible, then the rms value of the PCM52/53 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM52/53 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM52/53 the test period was chosen to be 22.7μsec (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, -20dB, and -60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

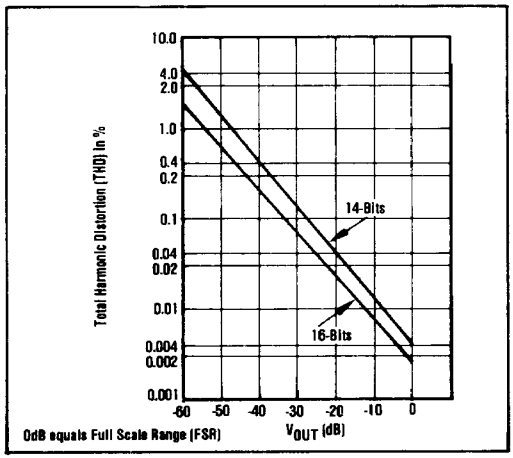


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

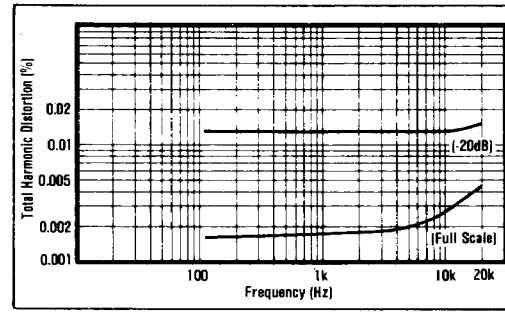


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

DIGITAL INPUT CODES

The PCM52/53 accepts complementary digital input codes in binary format. It may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
	MSB LSB	COB	CTC*
		Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 pin 1 to obtain CTC input code.

DETAILED THEORY OF OPERATION

In the basic design, the three functions represented by the complete D/A converter—the voltage reference, the output amplifier, and the converter—are distributed among six major circuit blocks (Figure 6). Three blocks—the open loop reference, the current-offset circuit, and the reference output amplifier—perform the reference functions. The D/A conversion is performed by two circuits called the upper converter and the lower converter, which are combined into the voltage output by the on-chip output op amp.

The prime requirements for a D/A converter circuit designed for PCM audio applications are that it have low differential linearity error and monotonicity and that it stay that way over a useful temperature range. To obtain this performance at 14 to 16 bits, the converter combines segmentation with multiple R-2R networks.

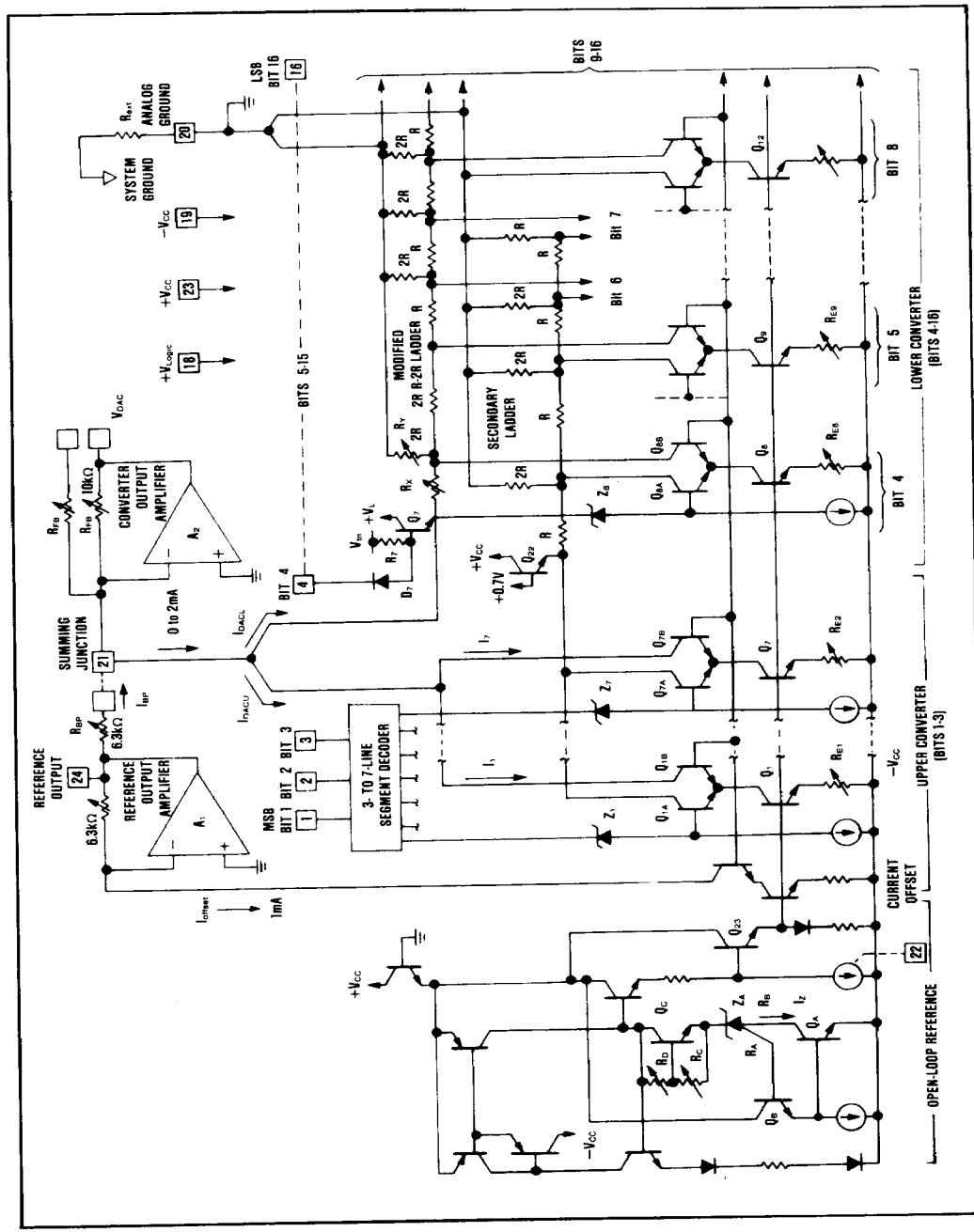


FIGURE 6. Simplified Circuit Diagram of the PCM52/53 16-bit Digital-to-Analog Converter.

The upper converter, which generates the three most significant bits, is made up of seven equal current sources (Q_1 R_{E1} through Q_1 R_{E7}), each providing 0.25mA. Together the sources form the upper converter current, I_{DACU}.

The three binary-coded MSBs (bits 1, 2, and 3) are decoded by a three-to-seven-line circuit, which sequentially selects the equal current sources as the binary code formed by the bits changes through the eight values (000 to 111). Thus, as the code ranges through its values, I_{DACU} changes from 0 to 1.75mA. This scheme ensures monotonicity, reduces initial matching and tracking requirements, and cuts the tracking errors that occur with temperature and time.

Averaging Transistor and Resistor Shifts

To further improve the tolerance of the upper converter to time and temperature change, the seven equal currents are turned on in the following order: Q_4, Q_2, Q_7, Q_5, Q_1, Q_6, Q_3. This sequence, which produces the zero-to-full-scale output, averages the shifts that occur in transistor parameters and in the value of the emitter resistors.

The 13 least significant bits are produced by the lower converter, which uses nine more equal-current sources for the nine middle bits and emitter area rationing for the 4LSBs. However, rather than being summed directly by the current of the upper converter (which would have required $2^{16}-1$ equal current sources) the current sources are further divided binarily by a pair of R-2R networks, called the modified R-2R ladder and the secondary ladder. By diverting the LSB currents through the modified ladder, the lower converter produces I_{DACL}. This current consists of $2^{13}-1$ discrete, 30nA steps for each 0.25mA segment of the upper converter. I_{DACU} and I_{DACL} are added at the summing junction, SJ, to form the I_{DAC}, which has a range that varies between 0 and 1.99997mA.

The modified R-2R ladder is superior to a conventional R-2R ladder because its output can be increased or decreased by laser-trimming of its output resistors (R_X and R_Y). Such trimming does not change the binary current division in the ladder. The gain of the lower converter can then be trimmed relative to the gain of the upper converter without interacting or in any way affecting the linearity of the lower converter.

The initial values of the 16 current sources are determined by the voltage at the output of the reference (the emitter of Q_{23}), but the sources are set to the same value when the emitter resistors (R_1-R_{16}) are laser-trimmed. The sources are turned on and off by a differential switch pair (such as Q_{5A}-Q_{5B}) driven by the low-power Schottky TTL-compatible input circuit (typical of D_8, R_8, Q_8, Z_8). The input circuit provides the level translation.

Constant Power

To maintain 16-bit performance, the on-chip power dissipation—and therefore the chip temperature—must be kept constant during code changes. Therefore the current from both the ON side (Q_{1B}) and the OFF side (Q_{1A}) of each differential switch pair in the upper converter should come from $+V_{CC}$, rather than one from $+V_{CC}$ and one from ground. The ON side currents (when the bits are on) come from $+V_{CC}$ and flow through A_2 and the feedback resistor, R_{fb}, to the summing junction to form I_{DACU}. Transistor Q_{22} is used to provide the OFF side current with a similar path to $+V_{CC}$. In the lower converter, the secondary R-2R ladder, which is connected between the OFF side of the differential switches and Q_{22}, provides the same function by keeping the $+V_{CC}$ current and the analog ground current constant with code changes.

The secondary ladder also significantly reduces linearity errors that would otherwise be caused by external ground wiring. Indeed, the secondary ladder makes possible the use of a single ground pin, which is the only way to make all the connections in a 24-pin package.

Most converters use a closed-loop op amp for precision DC biasing of their current sources. However, switching transients can cause excessive settling time in the op amp. To ensure minimum settling time, the PCM52/53 uses an open-loop reference circuit, which incidentally does not require space-consuming capacitors for frequency compensation or suppression of switching transients.

The reference voltage is generated by a Kelvin-sensed buried zener diode. Kelvin sensing is used because the elements of the buried zener, R_A and R_B, have a large and nonlinear temperature coefficient. The Kelvin-sensed connection removes from the reference path the large voltage drop, R_BI_Z, caused by the 1mA zener current I_Z. Instead it substitutes the voltage drop produced across R_A by the base current of Q_B.

Since this base current is only 1μA, the drop is negligible, and the true zener breakdown, V_Z is sensed. In addition great care was taken to ensure that all temperature-sensitive parts of the open-loop reference were laid out along lines of thermal equilibrium, to prevent thermal settling tails.

High-Speed Output Amplifier

The converter's output amplifier, A_2, which sums all of the output currents and converts them into the output voltage, V_{DAC}, must be just as accurate as the reference and current sources and just as fast as the switching circuits.

The amplifier is very fast, and it is well behaved when driving a capacitive load. It slews at 10V/μsec and typically settles to 0.003% of final value in less than 4μsec for a 20V step. For a step of 1LSB at the major carry, it settles in 1.5μsec. The thermal tails caused by temperature gradients and resistor self-heating are less than 0.001% of full scale.

Thermal tails occur when thermal gradients across the chip change as signal levels change. For example, when driving a load the output stage of the amplifier and its feedback resistor generate more heat at the full-scale output voltage than at zero. Therefore the temperature-

sensitive differential input stage, which is close by on the chip, uses cross-coupled transistors and resistors to equalize thermal gradients.

To achieve a ±10V output swing when operating from ±15V, the output stage of the amplifier uses two transistor pairs connected in series. This scheme is necessary because the breakdown voltage of the npn transistors is limited to 20V by the semiconductor process.

In addition, the output stage is biased in a class AB condition, so that current is always flowing. Continuous current flow is essential to ensure that the open-loop gain, A_O, and closed-loop output impedance, R_O, remain constant for both positive and negative full-scale output swings at 103dB and 0.03Ω, respectively. With lesser performance, errors would occur. If, for example, A_O changed from 94dB to 100dB for an output swing of −10V to +10V respectively, the output error would change by 100μV, and the change would be nonlinear. Likewise a nonlinear error approaching 200μV would occur if R_O changed from 0.04Ω to 0.08Ω.

DISCUSSION OF SPECIFICATIONS

The PCM52/53 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy. The PCM52/53 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is the deviation from zero volts out and is factory-trimmed to typically ±10mV at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 8.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM52/53 is factory-trimmed to typically ±0.001% of FSR.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM52/53 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM52/53 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM52/53 power supply sensitivity is specified for ±0.001% of FSR/%V_{CC} for all supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 7).

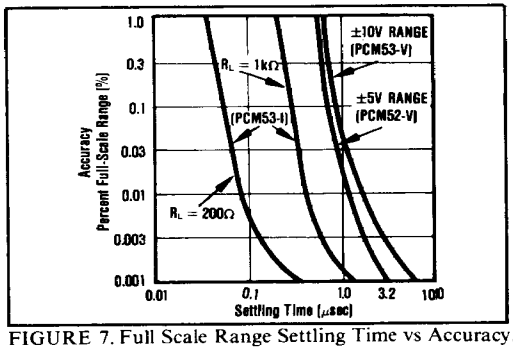


FIGURE 7. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM52/53.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the Bipolar Zero Error (offset) may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 8.

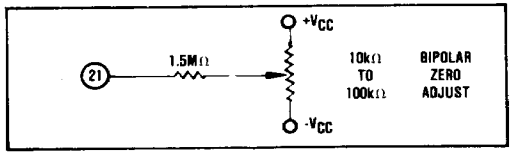


FIGURE 8. Optional External Bipolar Zero Adjust.

The potentiometer should have adequate resolution, at least 10 turns for full-scale resistance.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM52/53 to prevent noise pickup. Refer to Figure 9 for the relationship of Bipolar Zero adjust on the D/A converter transfer function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the bipolar zero potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V and ±5V output ranges.

INSTALLATION CONSIDERATIONS

If 14-bit resolution is desired, bit 15 (pin 15) and bit 16 (pin 16) should be connected to V_{DD} through a 1kΩ resistor to insure that these bits remain off.

Figure 10 shows the connection diagram for a PCM52/53-V. Figures 11 and 12 show connection diagrams for PCM53-I models.

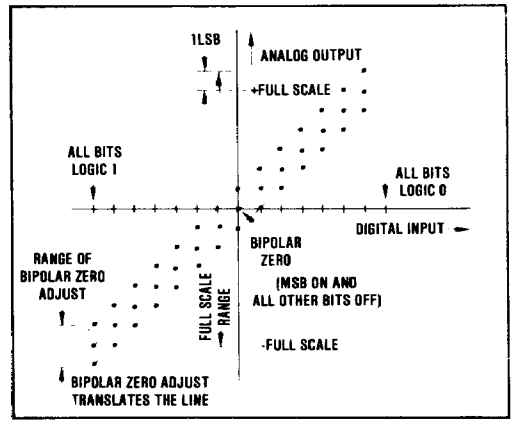


FIGURE 9. Effect of Bipolar Zero Adjustment on a Bipolar D/A Converter Transfer Function.

TABLE II. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODE	OUTPUT			
	Voltage Model		Current Model	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB)				
±10V (PCM53)				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On				
00...00	+9.99969V	+9.99878V	−0.99997mA	−0.99988mA
All Bits Off				
11...11	−10.00000V	−10.00000V	−1.00000mA	+1.00000mA
±5V (PCM52)				
One LSB	+152μV	+610μV		
All Bits On				
00...00	+4.999848V	+4.99939V		
All Bits Off				
11...11	−5.00000V	−5.00000V		

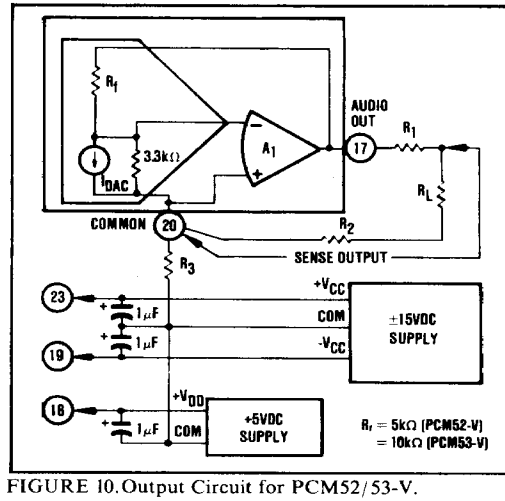


FIGURE 10. Output Circuit for PCM52/53-V.

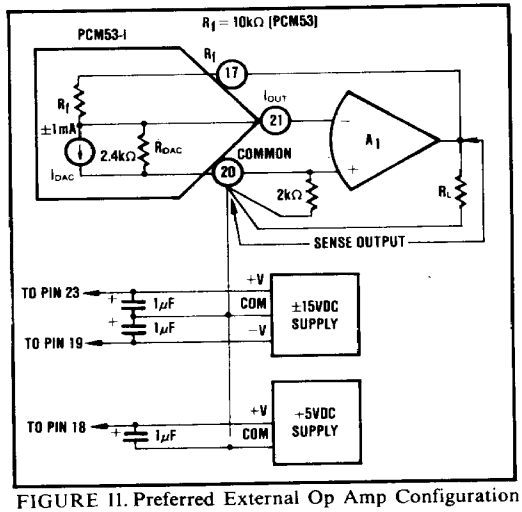


FIGURE 11. Preferred External Op Amp Configuration Using PCM53-I.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. R_L should be located as close as possible to the PCM52/53 for optimum performance.

The PCM52 53 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

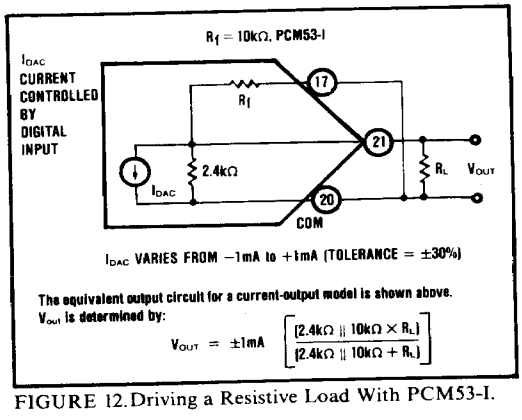


FIGURE 12. Driving a Resistive Load With PCM53-I.

The PCM52/53 is not normally sensitive to electrostatic discharge (ESD). Figures 11 and 12 show connection diagrams for PCM53-I models.

APPLICATIONS

Figures 13 and 14 show a circuit diagram and timing diagram of a single PCM52/53-V used to obtain both left and right channel audio output in a typical digital audio system. The Sony CX-7934 and associated LSI logic contain all of the required circuitry for error detection, correction, and formatting of the digital data obtained from the Compact Disc prior to sending this information to the D/A converter. The CX-7934 is used in a parallel output mode where the left and right channel parallel data are time-shared. Since the digital inputs of the PCM52/53 are TTL-compatible, they can be connected directly to the parallel outputs of the CX-7934. Only a single inverter is required (Bit 1) to convert the two's complement output code of the CX-7934 to offset binary. The audio output of the PCM52/53-V is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM52/53-V is a complete D/A converter.

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 15. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{on} by the audio signal.

Figure 16 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μsec ($t\omega$) is provided to eliminate the glitch and allow the output of the PCM52/53-V to settle within a small error band around its final value before connecting it to the channel output.

Due to the fast settling time of the PCM52/53-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

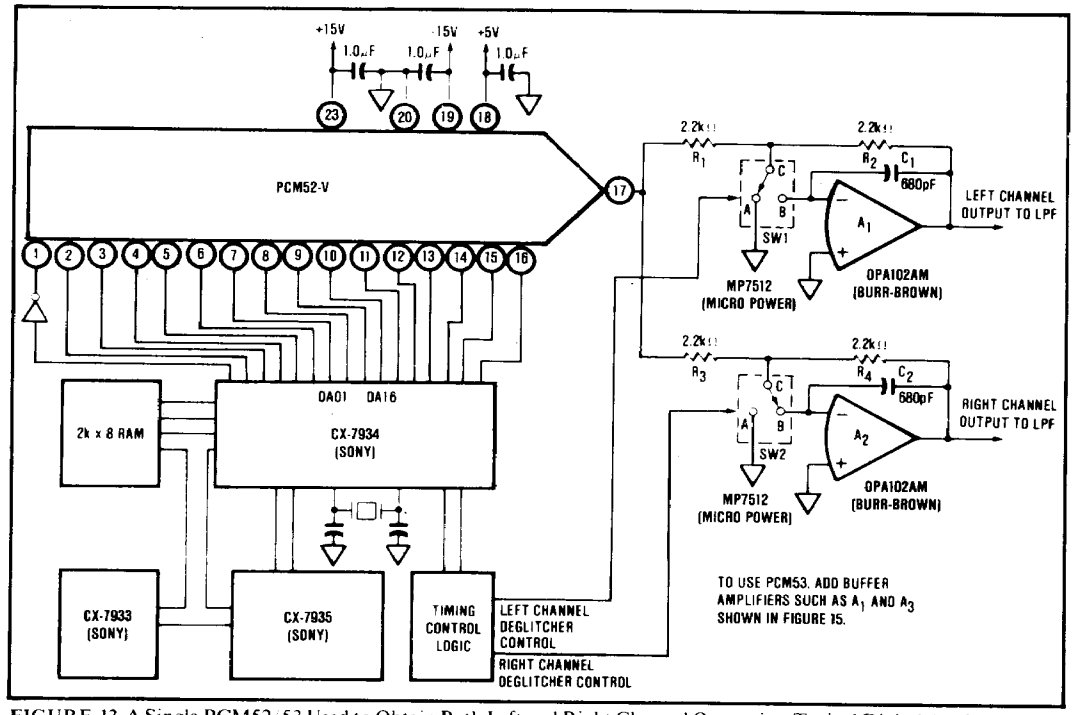


FIGURE 13. A Single PCM52/53 Used to Obtain Both Left and Right Channel Output in a Typical Digital Audio System.

SECOND-GENERATION SYSTEMS

One method of avoiding this problem and obtaining a linear phase response is to use an oversampling digital filter technique as shown in Figure 17. The Yamaha YM-3511 and YM-2201 LSI chips provide all of the functions described for the Sony chip set and, in addition, contain an onboard digital oversampling filter which effectively multiplies the sampling frequency by a factor of two and sends the parallel data at a rate of 88.2kHz to the D/A converter. Since the offset binary parallel data is directly available from the YM-2201, no external inverter is required. Furthermore, since the deglitcher control signal is also available from the YM-2201, no external timing control logic is required for most applications. The timing diagram for this circuit is shown in Figure 18.

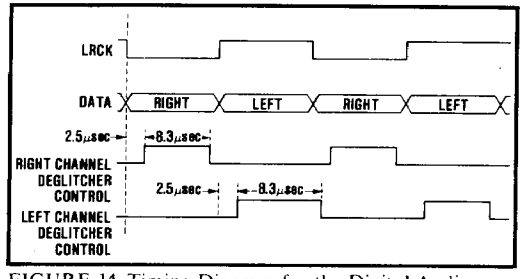


FIGURE 14. Timing Diagram for the Digital Audio System using PCM52/53 and Sony LSI Logic.

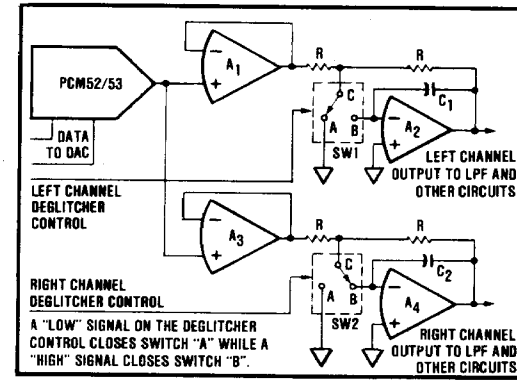


FIGURE 15. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

This circuit requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more. This technique results in intermodulation products being created, by mixing the sampling frequency and components of the audio frequency, that are far outside the audio band of 0 to 20kHz. These unwanted frequencies

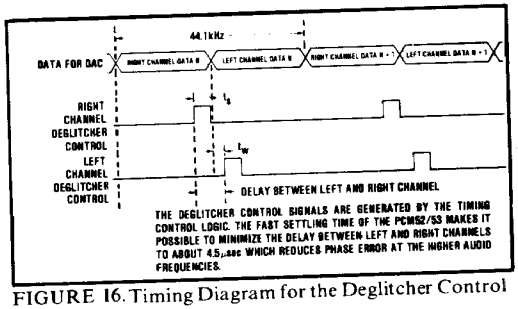


FIGURE 16. Timing Diagram for the Deglitcher Control Signals.

are easily removed by a low-order linear-phase analog filter following the deglitcher circuit since a sharp amplitude response is not required. A single PCM52/53-V can be used for both the left and right channel as long as the oversampling rate of the digital filter is two. An oversampling rate of four can be used if a separate PCM52/53 is used for each channel. This would reduce the complexities of the analog filter required even further (at the expense of an additional D/A converter).

Another factor to consider when choosing a D/A converter for digital audio applications is that the linearity of the total harmonic distortion versus output signal should be good since a change in the background noise level can be audible. The design of the PCM52/53 ensures that the linearity of the total harmonic distortion versus output signal level is very good over the full range of amplitude and frequencies. Also, no special grounding or shielding techniques are required to obtain good signal-to-noise ratio with the PCM52/53. Some converters require a high frequency clock which can couple to the analog output of the D/A converter through the output wiring and ground circuitry.

The PCM52 and PCM53 D/A converters provide a complete solution to one of the most critical portions of a digital audio system. Since the sound of the system can be affected by the D/A converter more than any other single component, the selection of which converter to use should be made with care.

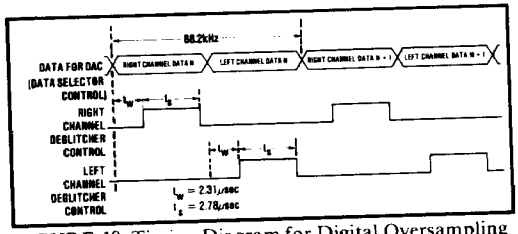


FIGURE 18. Timing Diagram for Digital Oversampling Technique when using Yamaha LSI.

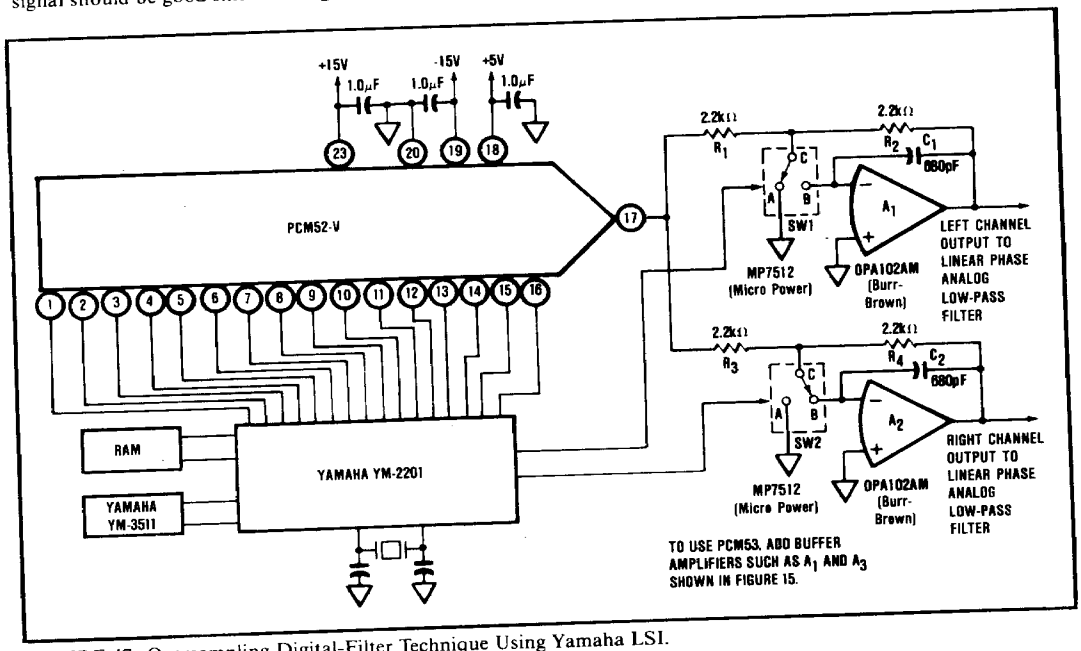


FIGURE 17. Oversampling Digital-Filter Technique Using Yamaha LSI.