o Outline

. The MN6471 is an 18-bit D/A converter, incorporating a digital filter (16-bit digital filter input), which was developed for the PCM digital audio equipment.

. A digital signal is output as the PWM signal by using the MASH system (Note 1).

. A built-in digital filter for fourfold oversampling provides a simplified low pass filter and largely reduced power consumption of the entire D/A conversion system.

. Two built-in channels have the positive phase and negative phase outputs respectively.

. The 4 D/A converter configuration using the differential circuit can realize a low distortion rate and a high S/N ratio.

. Substantial economization and miniaturization can be achieved by using this converter for the digital AV equipment such as CD players.

(Note 1) Requiring no processing step such as trimming through the cascade connection of the requantizer to the multi-stages, the MASH system is the oversampling D/A converting technology most suitable for realizing a high S/N ratio.

* MASH (Multi-stage noise shaping) is originated by NTT (Nippon Telegraph and Telephone Corp.).

* NTT is applying for registration of MASH as its trademark.

o Features

. Fourfold oversampling digital filter built in
(Ripple within the band: 0.0072dB, Attenuation factor in the interrupting area: 62.7dB)

. 18-bit D.F output, 18-bit MASH resolution, 18-bit total resolution

. 2s complementary input (compatible with I²S input cord)

. Overflow limiter built in

. No zero cross distortion

. 4 D/A converter configuration possible

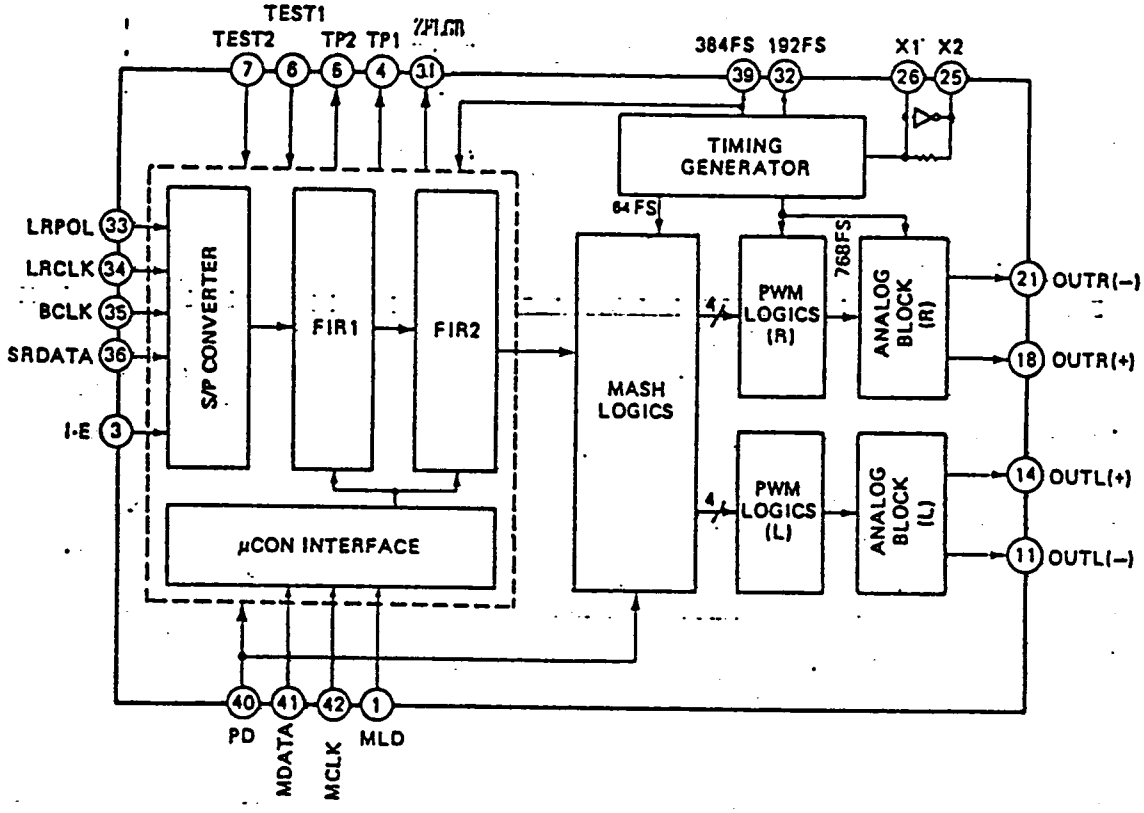
. Sample hold circuit not required

. Zero input detecting output pin available

. Size D 5V power supply

(Note) When using "MASH" for advertising of your set equipped with this LSI, be sure to state the following sentence.
"NTT is applying for registration of MASH as its trademark."

Block Diagram



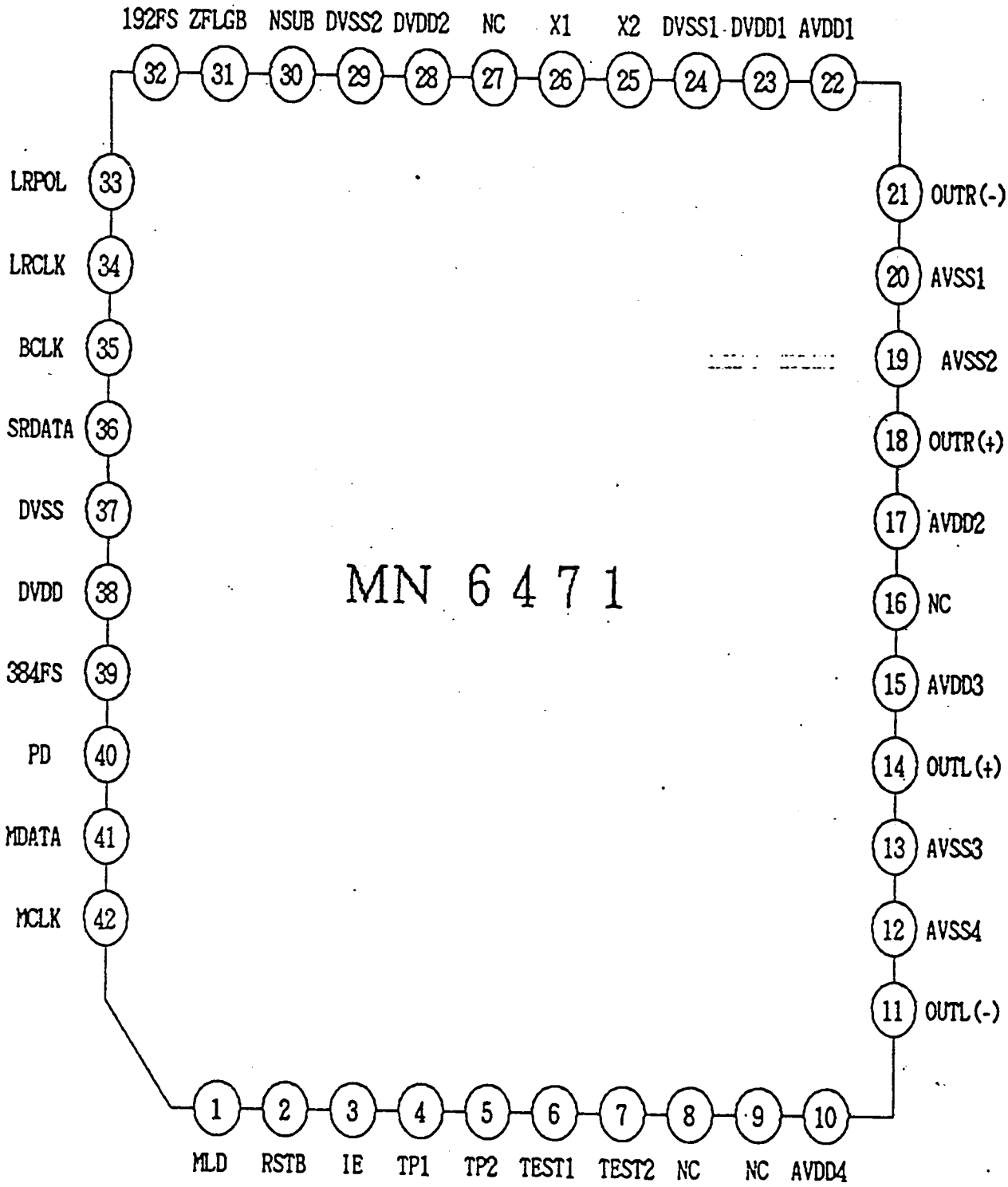
Pin Descriptions

No.	Pin Name	Descriptions
1	MLD	Microcomputer command load input (Load for L)
2	RSTB	Reset pin (Active for L)
3	IE	Signal processing LSI format for L , I^2S format for H
4	TP1	Digital filter test output pin 1
5	TP2	Digital filter test output pin 2
6	TEST 1	Digital filter checking test signal input pin 1 Usually "L"
7	TEST 2	Digital filter checking test signal input pin 2 Usually "L"
8	NC	———
9	NC	———
10	AVDD4	Analog power supply pin 4 (+5V)
11	OUTL(-)	L-ch negative phase PWM output pin
12	AVSS4	Analog ground pin 4
13	AVSS3	Analog ground pin 3
14	OUTL(+)	L-ch positive phase PWM output pin
15	AVDD3	Analog power supply pin 3 (+5V)
16	NC	———
17	AVDD2	Analog power supply pin 2 (+5V)
18	OUTR(+)	R-ch positive PWM output pin
19	AVSS2	Analog ground pin 2
20	AVSS1	Analog ground pin 1
21	OUTR(-)	R-ch negative phase PWM output pin

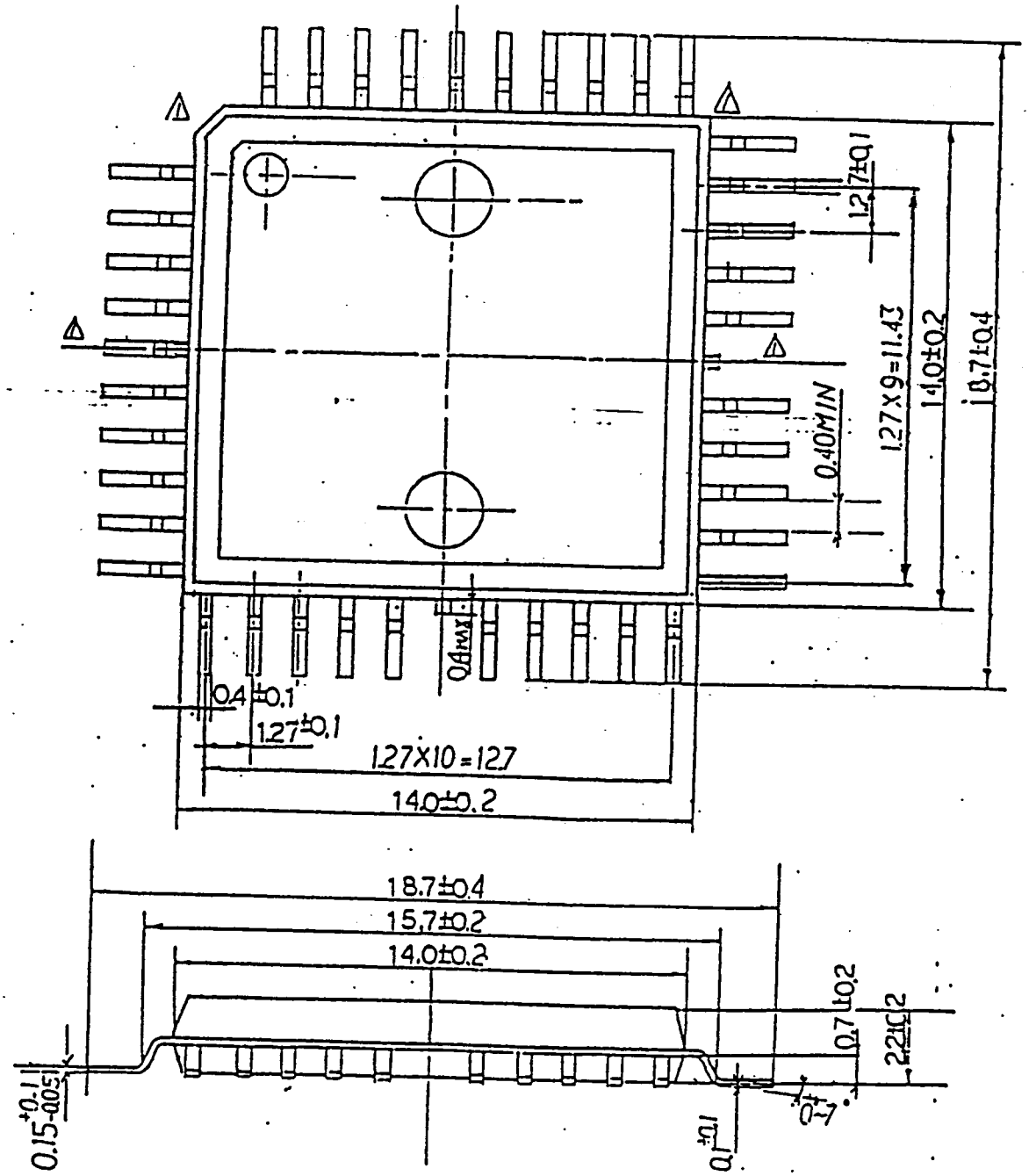
Pin Descriptions (continued)

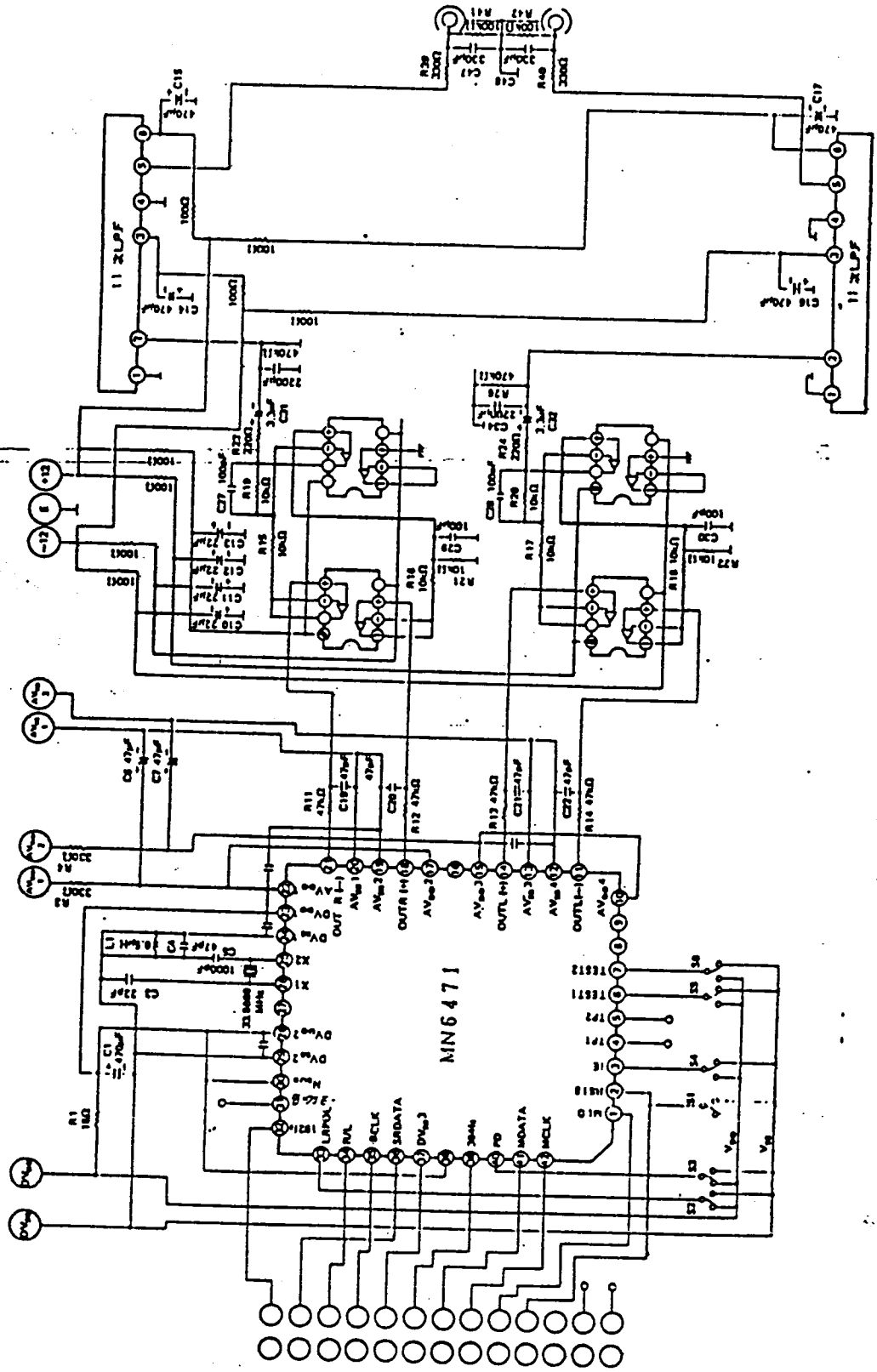
No.	Pin Name	Descriptions
22	AVVD1	Analog power supply pin 1 (+5V)
23	DVDD1	Digital power supply pin 1 (+5V) (Oscillation circuit power supply)
24	DVSS1	Digital ground pin 1 (Oscillation circuit ground)
25	X2	X'tal oscillation pin
26	X1	X'tal oscillation pin (External clock input pin)
27	NC	———
28	DVDD2	Digital power supply pin 2 (+5V)
29	DVSS2	Digital ground pin 2
30	NSUB	To be connected to D-VDD (Silicon PCB potential fixed pin)
31	ZFLGB	Zero input detection output pin
32	192FS	192FS (=8.4672MHz) output pin
33	LRPOL	LRCLK polarity switching pin (H L-ch, L R-ch)
34	LRCLK	LRCLK input pin For LR-POL H , H L-ch data input, L R-ch data input For LR-POL L , L L-ch data input, H R-ch data input
35	BCLK	Serial input bit clock
36	SRDATA	Serial input data (digital) input pin
37	DVSS3	Digital ground pin 3
38	DVDD	Digital power supply pin (COM potential fixed pin)(+5V)
39	384FS	384FS (=16.9344MHz) output pin
40	PD	Power-down pin (Active for H)
41	MDATA	Microcomputer command data input pin
42	MCLK	Microcomputer command clock input pin

Pin Configurations



Outline

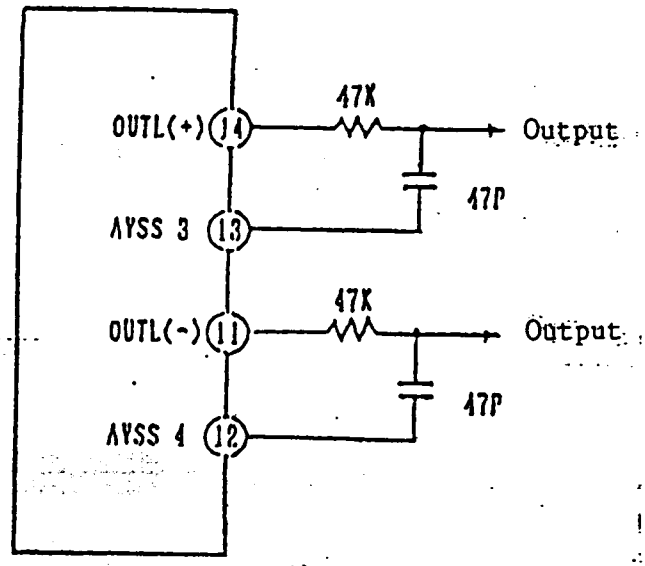

1.27±0.1
1.27X9=11.43
14.0±0.2
18.7±0.4
0.40MIN
0.4MAX
0.4±0.1
1.27±0.1
1.27X10=12.7
14.0±0.2
18.7±0.4
15.7±0.2
14.0±0.2
0.7±0.2
2.2±0.2
0.15+0.1-0.05
0.1±0.1
0°-7°



Example of Practical Circuit

Request for Designing

For improvement of quality (latch-up breakdown quantity), it is recommended to use the following low pass filter circuit.



* Same as R-ch

[OUTR(+) Pin 18]
[AVss2 Pin 19]

[OUTR(-) Pin 21]
[AVssl Pin 20]

(Connect at the root of LSI pin.)

* Because OUTL(-), OUTL(+), OUTR(+), and OUTR(-) pins are the high-precision analog output pin, be careful of handling for surge, etc.

Description

o Digital Attenuation

When 8-bit serial data is transmitted to MDATA, MCLK, and MLD at timing as shown in Fig. 1, the digital attenuation is applied corresponding to data value. Input is from MSB and upper 2 bits must always be 1 or 0. The attenuation level can be changed by changing the following 6-bit value. (Refer to Table 1.)

If RSTB is set to "L", the attenuation level setting latch circuit is reset and the attenuation level is 0dB. When RSTB is "L", the DF circuit stops the operation; thus, it is impossible to perform the attenuation operation with RSTB set to "L".

When MDATA is not transmitted, MGLK must be set to "H".

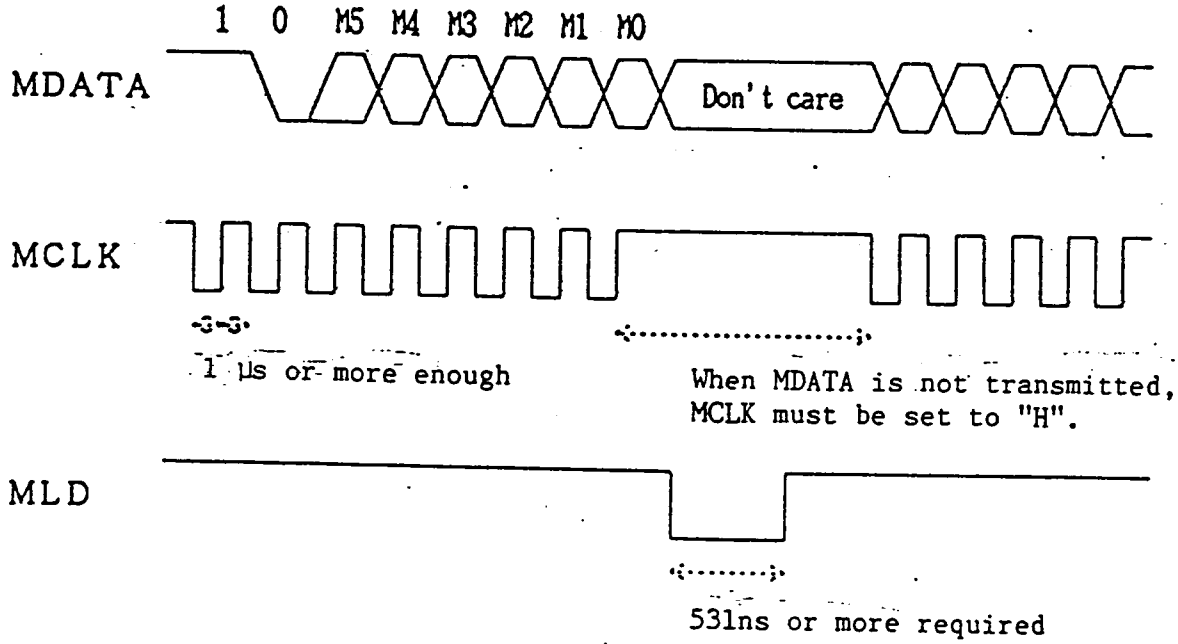


Fig. 1 Timing Chart

Table 1 MN6471 Digital Attenuation Level

MDATA MSB M5 M4 M3 M2 M1 LSB M0	Attenuation level (dB)	MDATA MSB M5 M4 M3 M2 M1 LSB M0	Attenuation level (dB)
1 0 0 0 0 0 0 0	0	1 0 1 0 0 0 0 0	- 6.30
1 0 0 0 0 0 0 1	- 0.28	1 0 1 0 0 0 0 1	- 6.58
1 0 0 0 0 0 1 0	- 0.42	1 0 1 0 0 0 1 0	- 6.88
1 0 0 0 0 0 1 1	- 0.56	1 0 1 0 0 0 1 1	- 7.18
1 0 0 0 0 1 0 0	- 0.71	1 0 1 0 0 1 0 0	- 7.50
1 0 0 0 0 1 0 1	- 0.86	1 0 1 0 0 1 0 1	- 7.82
1 0 0 0 0 1 1 0	- 1.01	1 0 1 0 0 1 1 0	- 8.16
1 0 0 0 0 1 1 1	- 1.16	1 0 1 0 0 1 1 1	- 8.52
1 0 0 0 1 0 0 0	- 1.32	1 0 1 0 1 0 0 0	- 8.89
1 0 0 0 1 0 0 1	- 1.48	1 0 1 0 1 0 0 1	- 9.28
1 0 0 0 1 0 1 0	- 1.64	1 0 1 0 1 0 1 0	- 9.68
1 0 0 0 1 0 1 1	- 1.80	1 0 1 0 1 0 1 1	-10.10
1 0 0 0 1 1 0 0	- 1.97	1 0 1 0 1 1 0 0	-10.55
1 0 0 0 1 1 0 1	- 2.14	1 0 1 0 1 1 0 1	-11.02
1 0 0 0 1 1 1 0	- 2.32	1 0 1 0 1 1 1 0	-11.51
1 0 0 0 1 1 1 1	- 2.50	1 0 1 0 1 1 1 1	-12.04
1 0 0 1 0 0 0 0	- 2.68	1 0 1 1 0 0 0 0	-12.60
1 0 0 1 0 0 0 1	- 2.87	1 0 1 1 0 0 0 1	-13.20
1 0 0 1 0 0 1 0	- 3.06	1 0 1 1 0 0 1 0	-13.84
1 0 0 1 0 0 1 1	- 3.25	1 0 1 1 0 0 1 1	-14.54
1 0 0 1 0 1 0 0	- 3.45	1 0 1 1 0 1 0 0	-15.30
1 0 0 1 0 1 0 1	- 3.66	1 0 1 1 0 1 0 1	-16.12
1 0 0 1 0 1 1 0	- 3.87	1 0 1 1 0 1 1 0	-17.04
1 0 0 1 0 1 1 1	- 4.08	1 0 1 1 0 1 1 1	-18.06
1 0 0 1 1 0 0 0	- 4.30	1 0 1 1 1 0 0 0	-19.22
1 0 0 1 1 0 0 1	- 4.53	1 0 1 1 1 0 0 1	-20.56
1 0 0 1 1 0 1 0	- 4.76	1 0 1 1 1 0 1 0	-22.14
1 0 0 1 1 0 1 1	- 5.00	1 0 1 1 1 0 1 1	-24.08
1 0 0 1 1 1 0 0	- 5.24	1 0 1 1 1 1 0 0	-26.58
1 0 0 1 1 1 0 1	- 5.49	1 0 1 1 1 1 0 1	-30.10
1 0 0 1 1 1 1 0	- 5.75	1 0 1 1 1 1 1 0	-36.12
1 0 0 1 1 1 1 1	- 6.02	1 0 1 1 1 1 1 1	- ∞

Type	MOS Silicon LSI
Function	Digital Filter + DA Converter (Digital audio LSI)
Connection	Fig. 1
Outline	Fig. 2

A. Absolute Maximum Rating

	Item	Symbol	Rating	Unit	Remarks
A1	Power supply voltage	D-VDD A-VDD	-0.3 ∿ +7.0	V	D-VSS=0V A-VSS=0V
A2	Input voltage	VI	D-VSS-0.3 ∿ D-VDD+0.3 A-VSS-0.3 ∿ A-VDD+0.3	V	"
A3	Output voltage	VO	D-VSS-0.3 ∿ D-VDD+0.3 A-VSS-0.3 ∿ A-VDD+0.3	V	"
A4	Power dissipation	Pd	300	mW	"
A5	Operating ambient temperature	Topr	-20 ∿ +70	C	
A6	Storage temperature	Tstg	-55 ∿ +125	C	

* The tentative product specifications are subject to change for revision without prior notice.

B. Operating Conditions

Ta=-20°C ∿ 70°C

	Item	Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
B1	Digital power supply voltage	D-VDD		4.50	5.0	5.50	V
B2	Analog power supply voltage	A-VDD		4.50	5.0	5.50	V
B3	Self-excitation oscillation	f			33.8688		MHz
	OSC input level						
B4	Voltage high level	VOSH	D-VDD=5V	3.5		D-VDD	V
B5	Voltage low level	VOSL		D-VSS		1.5	V
B6	Clock period	tWX			29.5		ns
B7	High level width	tWH		10			ns
B8	Low level width	tWL		10			ns

C. Electrical Characteristics

(1) DC Characteristics

D-VDD=4.50V ∿ 5.50V
A-VDD=4.50V ∿ 5.50V
Ta=-20°C ∿ 70°C, f=33.8688MHz

	Item	Symbol	Condi-tions	Limits			Unit
				Min.	Typ.	Max.	
C1	Digital power supply current	IDD(D)	No external load		36	50	mA
	Analog power supply current	IDD(A)			3	4	mA
C2	Power consumption	Pt			195	297	mW
Input pin (Note 1)							
C3	Input voltage high level	VINH		0.7D-VDD		D-VDD	V
C4	Input voltage low level	VINL		D-VSS		0.3D-VDD	V
C5	Input leak current	IINL				±10	μA
Output pin (Note 2)							
C6	Output voltage high level	VOH	IOH=-1mA	D-VDD-0.5			V
C7	Output voltage low level	VOL	IOL=1mA			0.5	V
Pin Capacitance							
C8	Input pin	CI	VIN=2V		4.0		PF
C9	Output pin	CO	DO=2V		10.0		PF

(NOTE 1) MLD, RSTB, IE, TEST1, TEST2, LPPOL, LRCLK, BCLK, SRDATA, PD, MDATA, MCLK

(NOTE 2) TP1, TP2, OUTL(-), OUTL(+), OUTR(-), OUTR(+), 192FS, 384FS

D. AC Characteristics

D-VDD=4.50V ∿ 5.50V D-VSS=0V
A-VDD=4.50V ∿ 5.50V A-VSS=0V
Ta=-20°C ∿ 70°C, f=33.8688MHz

	Item	Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
	Data input						
D1	Data pulse width	tDW		240			ns
D2	Data hold time	tDH		100		tDW-100	ns
D3	BCLK period	tCBCLK		240			ns
D4	BCLK"H" pulse width	tHBCLK		100			ns
D5	BCLK"L" pulse width	tLBCLK		100			ns
D6	LRCLK edge from the rise of BCLK	tBLR		100		tCBCLK -100	ns

E. AC Characteristics

D-VDD=4.50V ∿ 5.50V D-VSS=0V
A-VDD=4.50V ∿ 5.50V A-VSS=0V
Ta=-20°C ∿ 70°C, f=33.8688MHz

Item		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
	Attenuation						
E1	Data set-up time	tADS		300			ns
E2	Data hold time	tADH		300			ns
E3	MCLK"H" pulse width	tHMCLK		300			ns
E4	MCLK"L" pulse width	tLMCLK		300			ns
E5	Data load time	tADL		300			ns
E6	MLD"L" pulse width	tLMLD		600			ns
E7	MCLK rise time	tMR	0.3VDD-> 0.7VDD			50	
E8	MCLK fall time	tMF	0.7VDD-> 0.3VDD			50	

F. AC Characteristics

D-VDD=5.0V D-VSS=0V
A-VDD=5.0V A-VSS=0V
Ta=25°C f=33.8688MHz

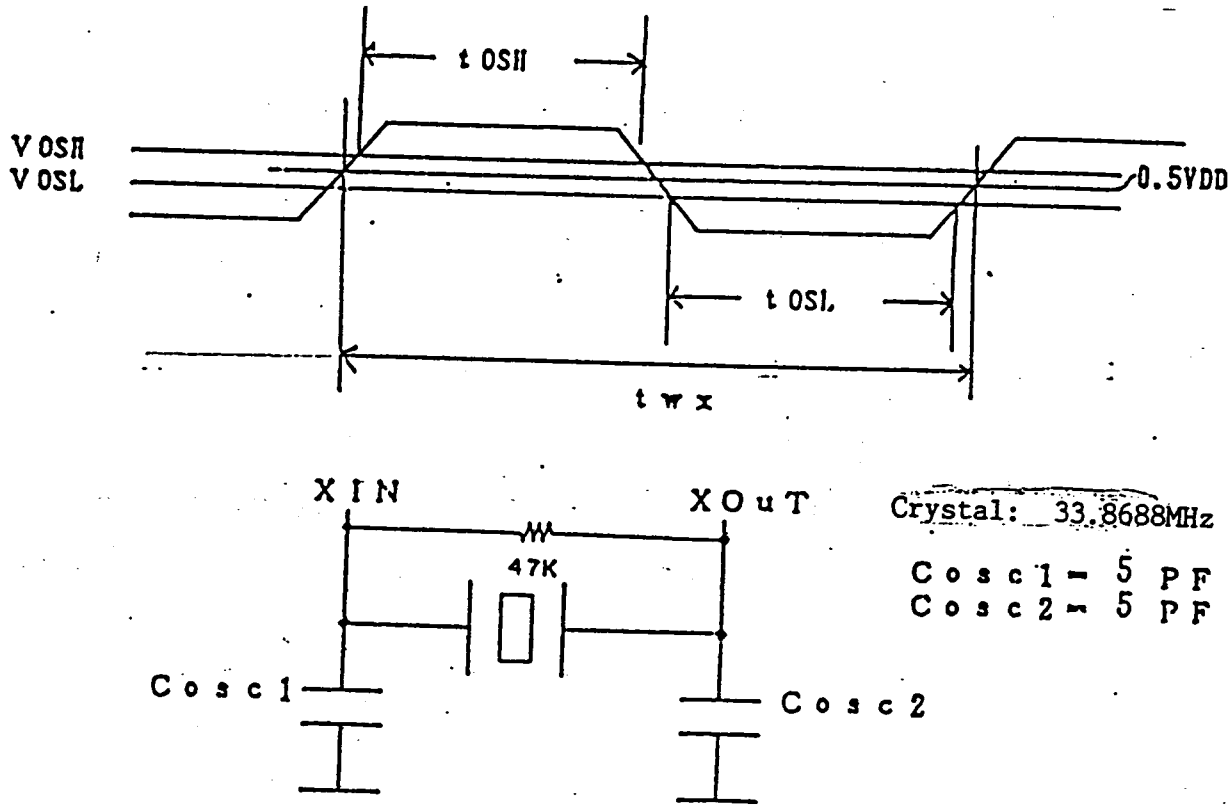
Item		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
Analog characteristics							
F1	Signal-to-noise ratio	S/N	EiAj	95	106		dB
F2	Dynamic range	D.R	"	90	98		dB
F3	Total harmonic distortion	THD	"		0.003	0.006	%
F4	Crosstalk		"	92	100		dB
F5	Output level (Note 1)		1KHz F.S.	1.4	1.7		Vrms

(Note 1) Differential circuit output

(Use the analog circuit equivalent to one in the example of practical circuit.)

Fig. 3

XIN input



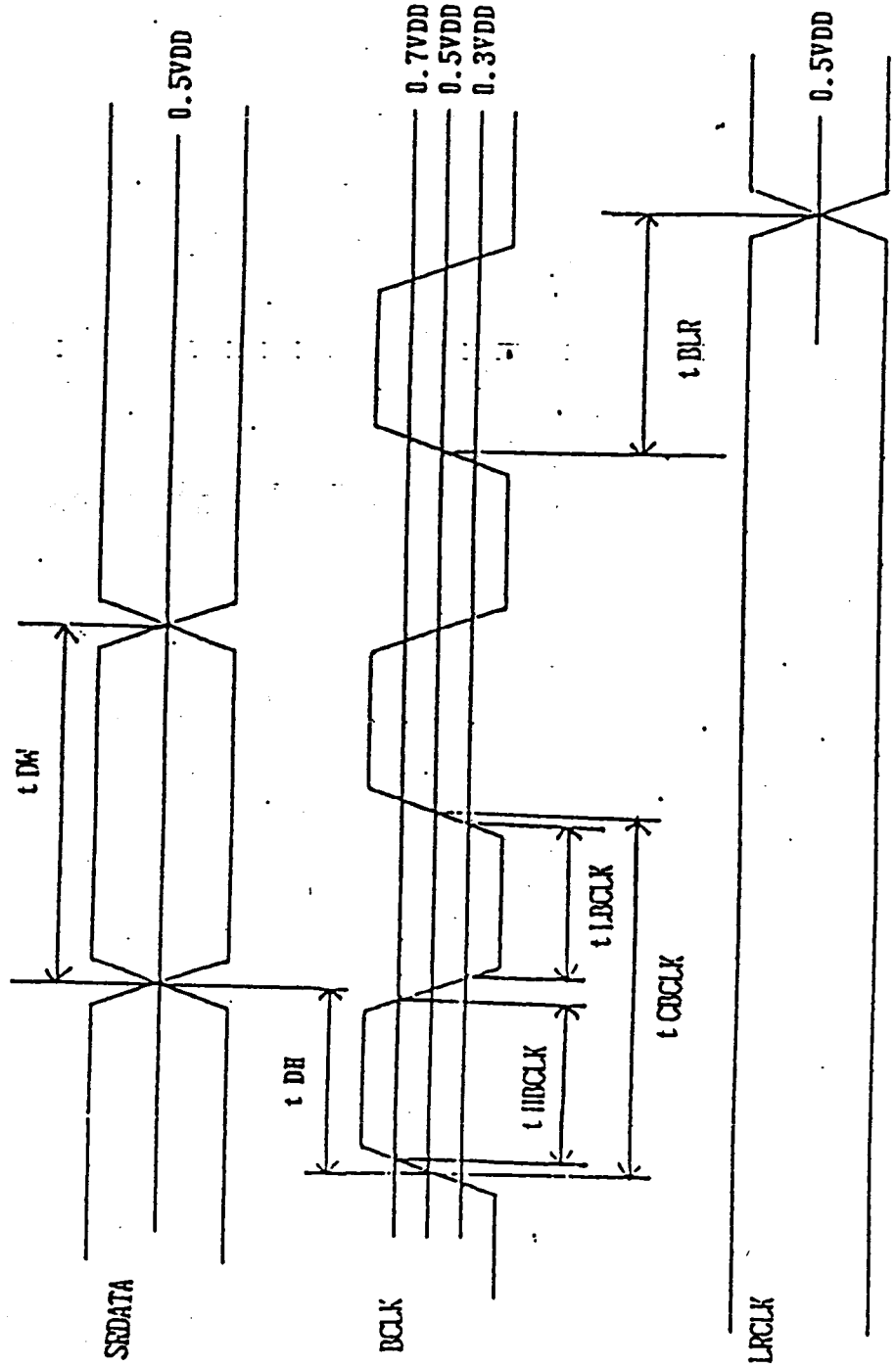

0.5VDD
0.7VDD
0.5VDD
0.3VDD
0.5VDD
tDW
tDH
tBLR
tIBCLK
tIIBCLK
tCDCLK
SRDATA
BCLK
LRCLK

Fig. 4

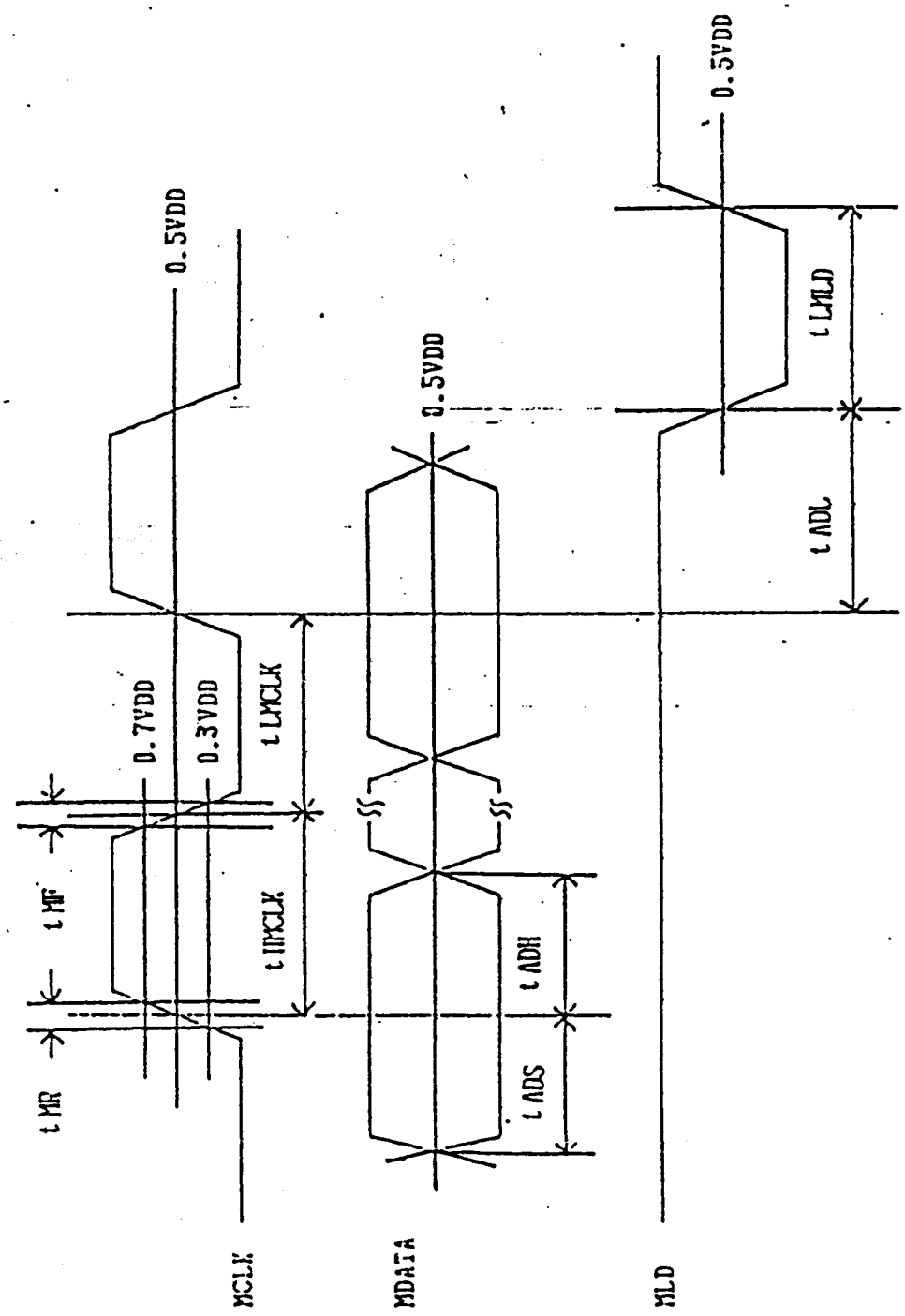

0.5VDD
0.5VDD
0.5VDD
0.7VDD
0.3VDD
tLMCLK
tLMLD
tADL
tMF
tIMCLK
tADH
tMR
tADS
MCLK
MDATA
MLD

Fig. 5