Ordering number: EN3861

CMOS LSI

SANYO No. 3861

LC78840M

Four-times or Eight-times Oversampling Digital Filter

OVERVIEW

The LC78840M is a four-times or eight-times oversampling digital filter for Broadcast Satellite (BS), Compact Disc (CD) and Digital Audio Tape (DAT) applications. The filter operates at 384fs, 392fs or 512fs, and has internal deemphasis for fs = 32, 44.1 or 48 kHz. Output data length is 18 or 16 bits for eight-times or four-times oversampling, respectively.

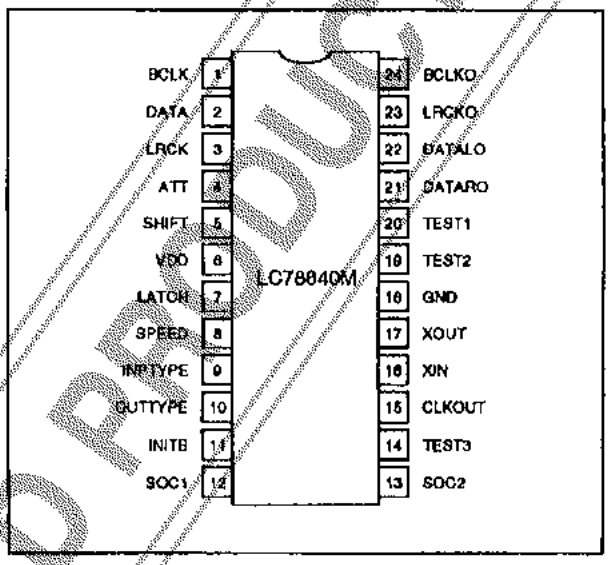
The LC78840M features a double-rate mode for dubbing CDs to cassette tape, where the data rate is doubled and the data is processed with half the oversampling of normal-rate mode. An external controller can be used to set the rate mode, output offset, deemphasis and attenuation.

The LC78840M operates from a 5 V supply and is available in 24-pin MFPs.

FEATURES

- Four-times or eight-times oversampling
- 384fs, 392fs and 512fs operation
- Double-rate compatible
- Selectable deemphasis
- Digital attenuator
- Optional output offset
- Two input and output formats
- 5 V supply
- 24-pin MFP

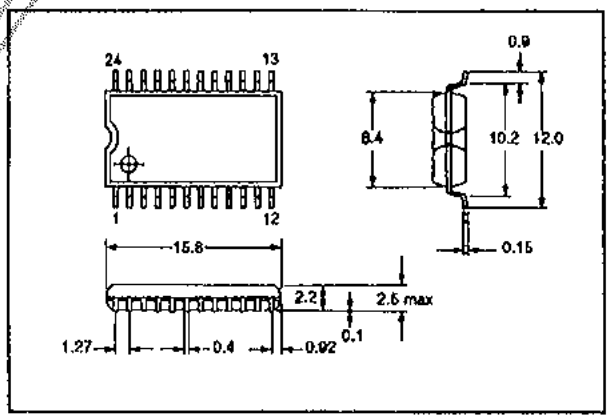
PINOUT



PACKAGE DIMENSIONS

Unit: mm

3155-MFP24



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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

PIN DESCRIPTION

Number	Name	Description
1	BCLK	Bit-clock input
2	DATA	Digital audio data input
3	LRCK	LR clock input
4	ATT	Attenuation data input. Normal/double-rate select in external set mode
5	SHIFT	Attenuation data shift clock input. Deemphasis select input in external set mode
6	VDD	5 V supply
7	LATCH	Attenuation data latch clock input. Deemphasis select input in external set mode
8	SPEED	Four- or eight-times oversampling select input
9	INPTYPE	Input format select input
10	OUTTYPE	Output format select input
11	INITB	Initialization input
12	SOC1	Input source and external set mode select input 1
13	SOC2	Input source and external set mode select input 2
14	TEST3	Test input 3
15	CLKOUT	Clock output
16	XIN	Crystal oscillator input
17	XOUT	Crystal oscillator output
18	GND	Ground
19	TEST2	Test input 2. Input source select 2 in external set mode
20	TEST1	Test input 1. Input source select 1 in external set mode
21	DATARO	Right-channel data output
22	DATALO	Left- and right-channel alternating data output for four-times oversampling, and left-channel data output for eight-times oversampling
23	LRCKO	Left- and right-channel clock output
24	BCLKO	Bit-clock output

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage range	V_O	−0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	−30 to 75	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Recommended Operating Conditions

T_a = −30 to 75 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

Electrical Characteristics

V_{DD} = 5 V, T_a = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level input voltage	V_{IL}		−0.3	–	0.8	V
HIGH-level input voltage	V_{IH}		2.2	–	V_{DD} + 0.3	V
LOW-level output voltage	V_{OL}	I_O = ±4 mA	–	–	0.4	V
HIGH-level output voltage	V_{OH}	I_O = ±4 mA	3.0	–	–	V
CLKOUT output amplitude	V_O	f_X = 16.9344 MHz, C_L = 20 pF	1	–	–	V_{PP}
Power consumption	P_D	V_{XIN} = 1.6 to 3.5 V_{PP}, f_X = 16.9344 MHz	–	250	300	mW
Oscillator frequency	f_X		–	16.9344	25	MHz
BCLK input frequency	f_{BCK}		–	–	3.1	MHz
TEST1, TEST2 and TEST3 input pull-down resistance	R_{DOWN}		10	–	80	kΩ

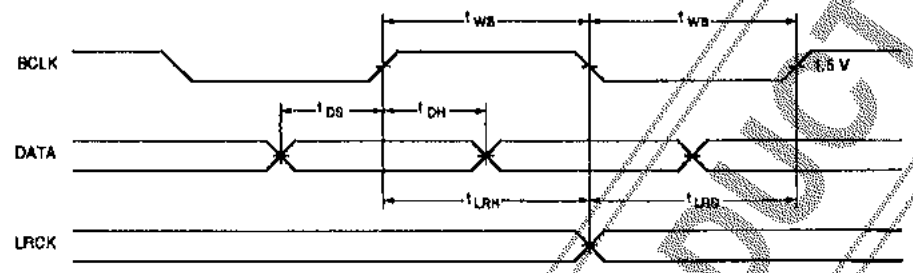
Timing Characteristics

V_{DD} = 5 V, T_a = 25 °C

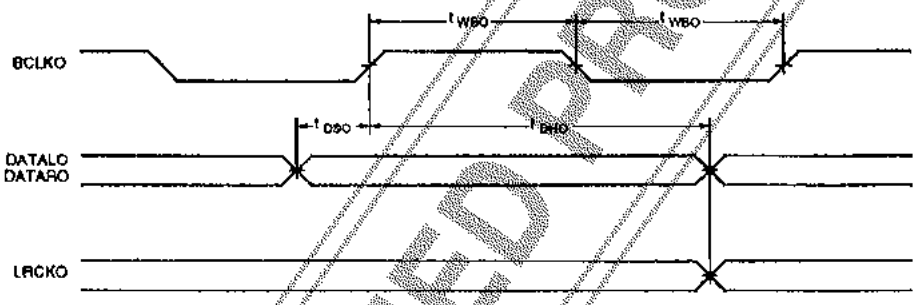
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCLK input pulsewidth	t_{WB}		100	–	–	ns
DATA input setup time	t_{DS}		20	–	–	ns
DATA input hold time	t_{DH}		20	–	–	ns
LRCK input setup time	t_{LRS}		50	–	–	ns
LRCK input hold time	t_{LRH}		50	–	–	ns
BCLKO output pulsewidth	t_{WBO}	Eight-times oversampling	40	–	–	ns
DATALO and DATARO output setup time	t_{DSO}	f_X = 16.9344 MHz	25	–	–	ns
DATALO and DATARO output hold time	t_{DHO}	C_L = 50 pF	25	–	–	ns
Program input reference time	t_{PR}	f_X = 16.9344 MHz	250	–	–	ns
LATCH input pulsewidth	t_{WLT}	f_X = 16.9344 MHz	50	–	–	ns
SHIFT and LATCH rise time	t_r		–	–	200	ns
SHIFT and LATCH fall time	t_f		–	–	200	ns

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
ATT input setup time	t_{SET}		500	–	–	ns
ATT input hold time	t_{HOLD}		500	–	–	ns
Interval time	t_{INT}		1000	–	–	ns

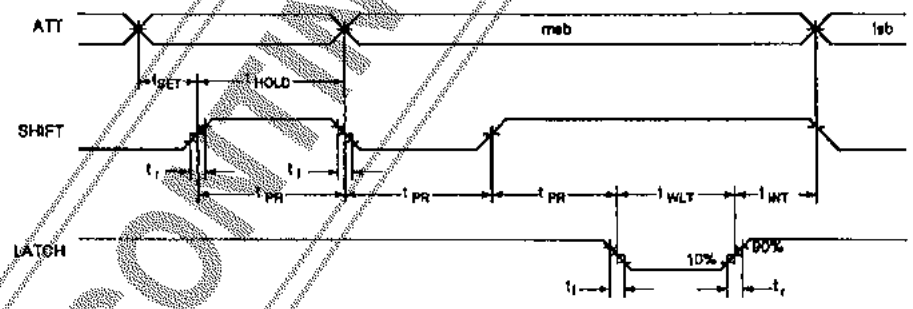
Audio Input



Audio output

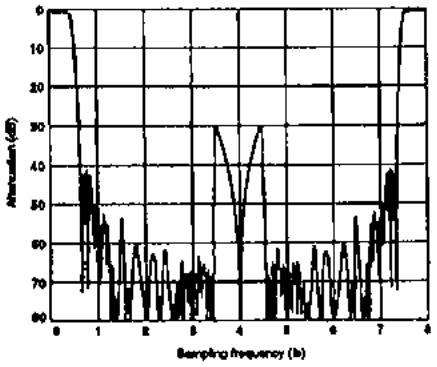


Program Input

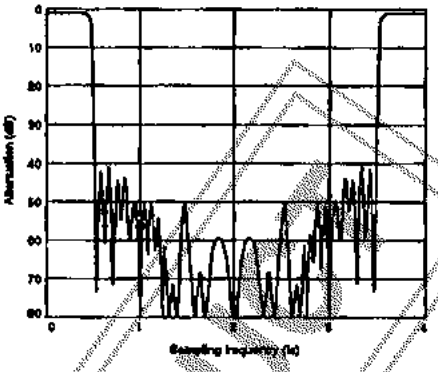


Theoretical Filter Response

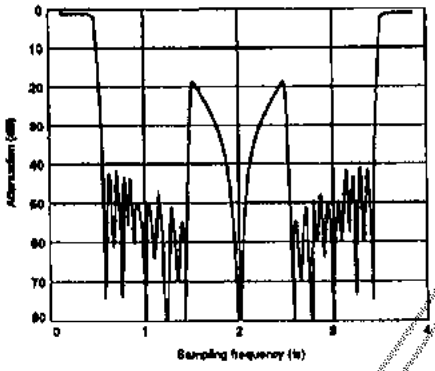
Normal-rate mode with eight-times oversampling



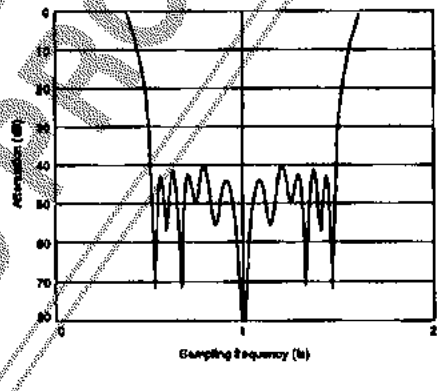
Normal-rate mode with four-times oversampling



Double-rate mode with eight-times oversampling



Double-rate mode with four-times oversampling



FUNCTIONAL DESCRIPTION

Eight-times Oversampling

In normal-rate mode, 43rd-order, 11th-order and 3rd-order FIR filters are used to successively generate data with two-times, four-times and eight-times oversampling, respectively, as shown in figure 1.

Deemphasis is performed by the 1st-order IIR filter. The least significant 4 bits of the 22-bit internal data are used for noise shaping. The output data length is 18 bits.

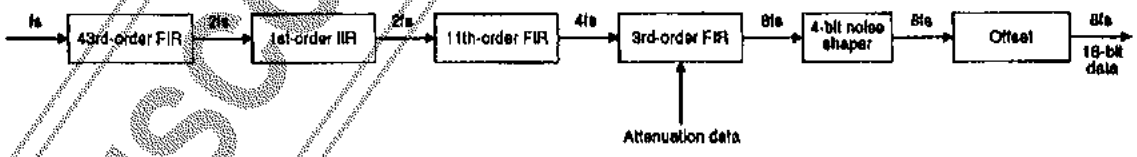


Figure 1. Normal-rate mode eight-times oversampling filter

Note

The offset is set ON or OFF by bit A0 of the input attenuation data. It adds 02AAH to the output data.

In double-rate mode, the filter operation is similar except that the 11th-order FIR filter is omitted, resulting in output data with four-times oversampling as shown in figure 2.

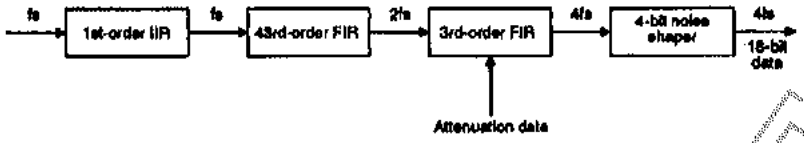


Figure 2. Double-rate mode eight-times oversampling filter

Note
fs is the double-rate input frequency.

Four-times Oversampling

In normal-rate mode, 43rd- and 11th-order FIR filters are used to successively generate data with two-times and four-times oversampling, respectively, as shown in figure 3.

Deemphasis is performed by the 1st-order IIR filter. The least significant 6 bits of the 22-bit internal data are used for noise-shaping. The output data length is 16 bits.

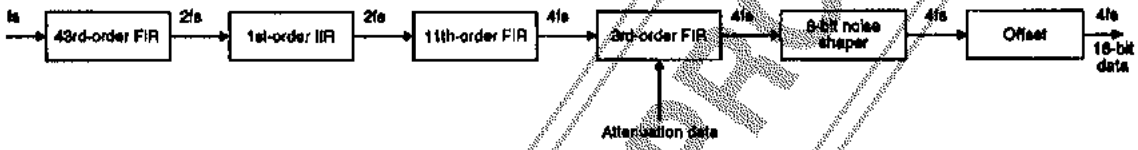


Figure 3. Normal-rate mode four-times oversampling filter

In double-rate mode, the filter operation is similar except that the 11th-order filter is omitted, resulting in output data with two-times oversampling as shown in figure 4.

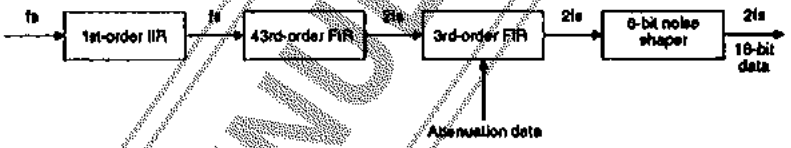


Figure 4. Double-rate mode four-times oversampling filter

Note
fs is the double-rate input frequency.

Initialization

Initialization is required at power-on and when the input source is changed. At initialization, the LC78840M requires XIN, BCLK and LRCK, stable V_{DD}, and INITB set LOW for more than one cycle of LRCK, as shown in figure 5. Note that the LC78840M should be re-initialized if the input data format fails. This may occur during channel selection if LRCK slips out of phase or if the digital input phase relationships change.

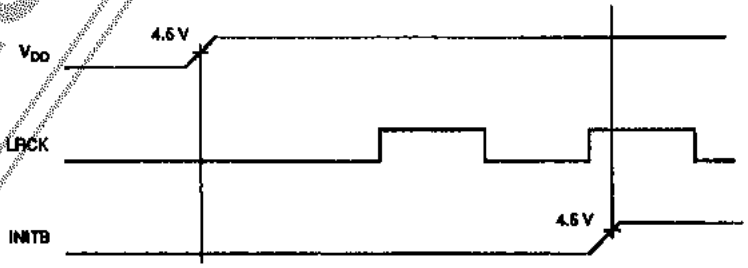


Figure 5. Initialization waveform

Pin Functions

SPEED

Set SPEED LOW for eight-times oversampling, or HIGH, for four-times oversampling.

INPTYPE

Set INPTYPE LOW for input data format A, or HIGH, for format B.

OUTTYPE

Set OUTTYPE LOW for output data format A, or HIGH, for format B.

TEST1, TEST2 and TEST3

These inputs have internal pull-down resistors and are normally LOW. In external set mode, TEST1 and TEST2 select the input source.

SOC1 and SOC2

The input sources selected by SOC1 and SOC2 are shown in table 1. External set mode is selected when both inputs are HIGH.

Table 1. SOC1 and SOC2 modes

SOC1	SOC2	Function	Input source
LOW	LOW	Input source select	384fs
LOW	HIGH		392fs
HIGH	LOW		512fs
HIGH	HIGH	External set mode	–

CLKOUT

The output frequency is $0.5f_X$ for a 392fs input source, or $0.25f_X$, for 384fs or 512fs input sources.

DATARO and DATALO

In eight-times oversampling mode, right-channel and left-channel data is output on DATARO and DATALO, respectively. In four-times oversampling mode, left-channel and right-channel data is output alternately on DATALO, and right-channel data only is output on DATARO.

External Set Mode

In this mode, the ATT data is not used. Instead, the selection of input source, deemphasis and normal- or double-rate is by the logic level controls on inputs, shown in tables 2 to 5.

Table 2. External set inputs

Input pin	Function
TEST1 TEST2	Selects input source in place of SOC1 and SOC2. See table 3.
ATT	Selects rate mode. See table 4.
SHIFT LATCH	Selects deemphasis. See table 5.

Table 3. TEST1 and TEST2 input source select

TEST1	TEST2	Input source
LOW	LOW	384fs
LOW	HIGH	392fs
HIGH	LOW	512fs

Table 4. ATT rate mode select

ATT	Rate mode
LOW	Normal rate
HIGH	Double rate

Table 5. SHIFT and LATCH deemphasis select

SHIFT	LATCH	Deemphasis	Sampling frequency	Application
LOW	LOW	OFF	–	–
LOW	HIGH	ON	fs = 32 kHz	BS, DAT
HIGH	LOW	ON	fs = 44.1 kHz	CD
HIGH	HIGH	ON	fs = 48 kHz	BS, DAT

OPERATING INFORMATION

The input and output data formats for four- and eight-times oversampling are shown in figures 6 to 10. Data input and output take 48, 49 or 64 bit-clock periods for 384fs, 392fs or 512fs operation, respectively.

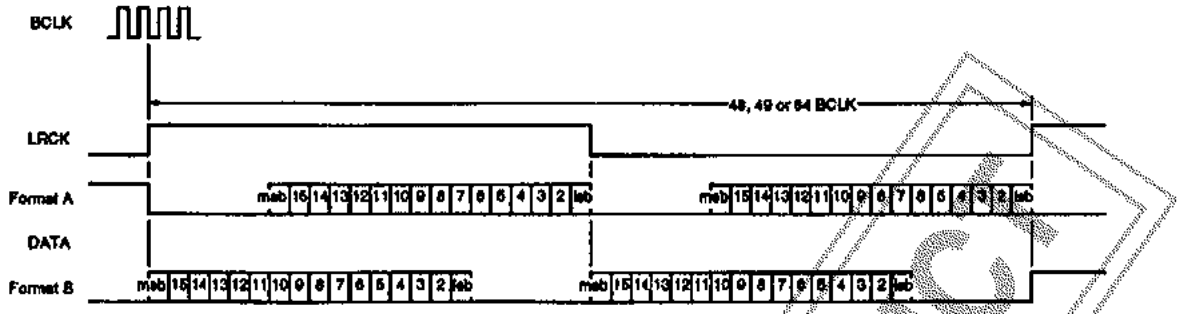


Figure 6. Input data format

Note

For 392fs operation, the LRCK mark-space ratio can be 24:25 or 25:24.

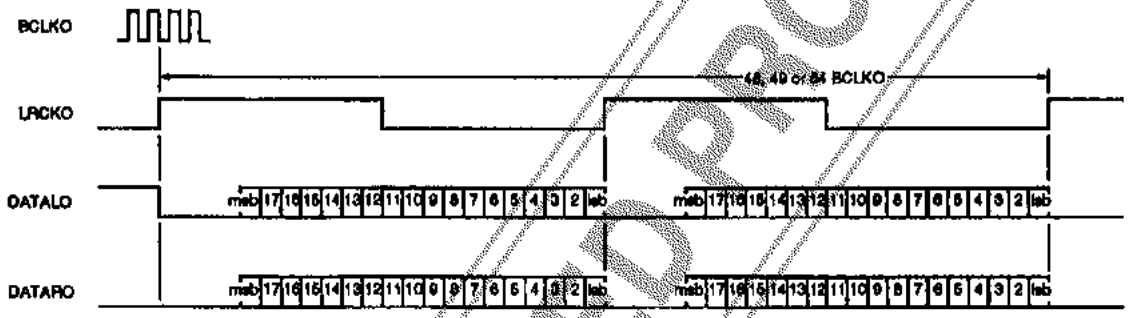


Figure 7. Eight-times oversampling, format A output data format

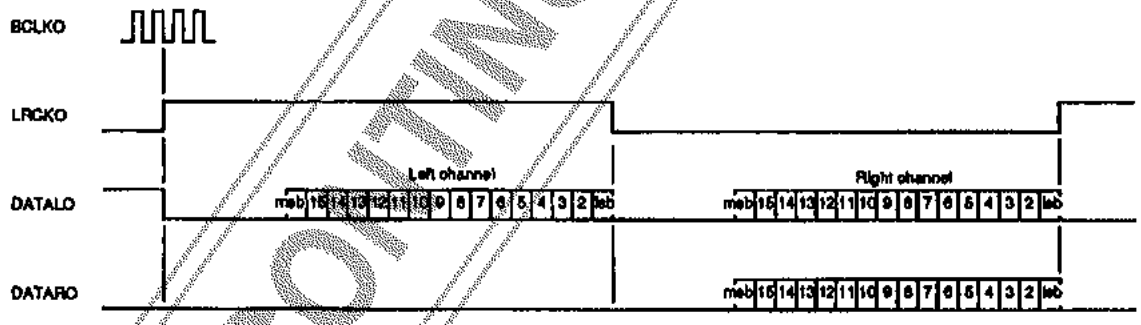


Figure 8. Four-times oversampling, format A output data format

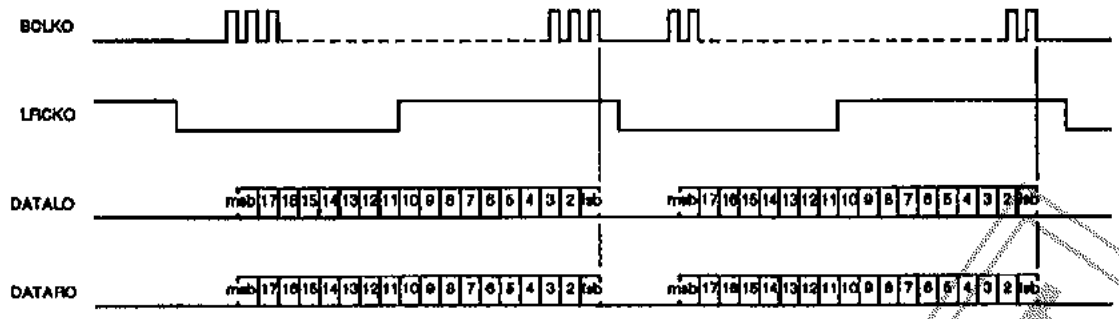


Figure 9. Eight-times oversampling, format B output data format

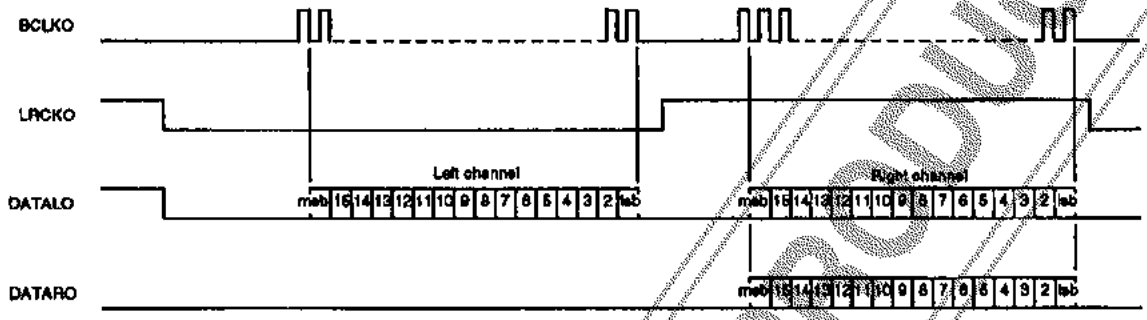


Figure 10. Four-times oversampling, format B output data format

Notes

1. The delay from data output to LRCKO is one BCLKO period.
2. For 392fs operation with 8-times oversampling, LRCKO has opposite phase for both A and B output formats.

DESIGN INFORMATION

ATT Data Format

Normal-rate or double-rate mode, deemphasis and filter attenuation can be set by data input on ATT. The data format is shown in figure 11. At initialization, the ATT register data is set to 4000H.

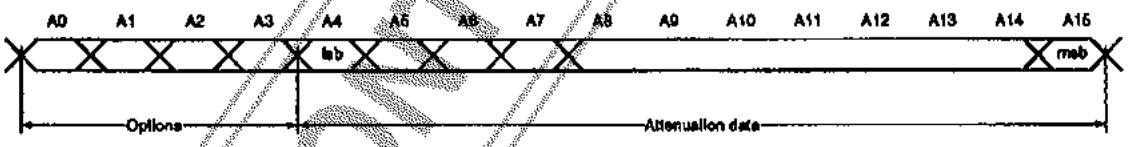


Figure 11. ATT data format

Attenuation data (A15 to A4)

A15 to A6 are the 10-bit attenuator multiplier coefficient, where the attenuation is given by the following equation.

$$\alpha_{multiplier} = 20 \times \log\left(\frac{A15 \text{ to } A6}{256}\right) dB$$

When A15 to A6 are all 0, A5 and A4 set further attenuation using a barrel shifter. The attenuation levels are shown in table 6.

Table 6. Attenuation levels

ATT attenuation data												Attenuation (dB)
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	
0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	0.034
0	0	1	1	1	1	1	1	1	1	1	0	0.034
0	0	1	1	1	1	1	1	1	1	0	1	0.034
0	0	1	1	1	1	1	1	1	1	0	0	0.034
0	0	1	1	1	1	1	1	1	0	1	1	0.068
0	0	1	1	1	1	1	1	1	0	1	0	0.068
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	0	0	0	1	0	0	48.16
0	0	0	0	0	0	0	0	0	0	1	1	50.66
0	0	0	0	0	0	0	0	0	0	1	0	54.19
0	0	0	0	0	0	0	0	0	0	0	1	60.21
0	0	0	0	0	0	0	0	0	0	0	0	∞

When the attenuation data is changed from 400H to 000H, the LC78840M performs software mute and ramps to infinite attenuation in 1024/fs seconds.

Options (A3 to A0)

A1 is the speed flag. When A1 = 0, normal-rate mode is selected, and when A1 = 1, double-rate mode is selected.

A0 is the offset flag. When A0 = 0, no offset is selected.

A2 and A3 select the deemphasis setting, as shown in table 7.

Table 7. A2 and A3 deemphasis select

A2	A3	Deemphasis	Sampling frequency	Application
0	0	OFF	–	–
0	1	ON	fs = 32 kHz	BS, DAT
1	0	ON	fs = 44.1 kHz	CD
1	1	ON	fs = 48 kHz	BS, DAT

TYPICAL APPLICATION

A typical application with eight-times oversampling, format A input and output data, and attenuation set by a CPU, is shown in figure 12.

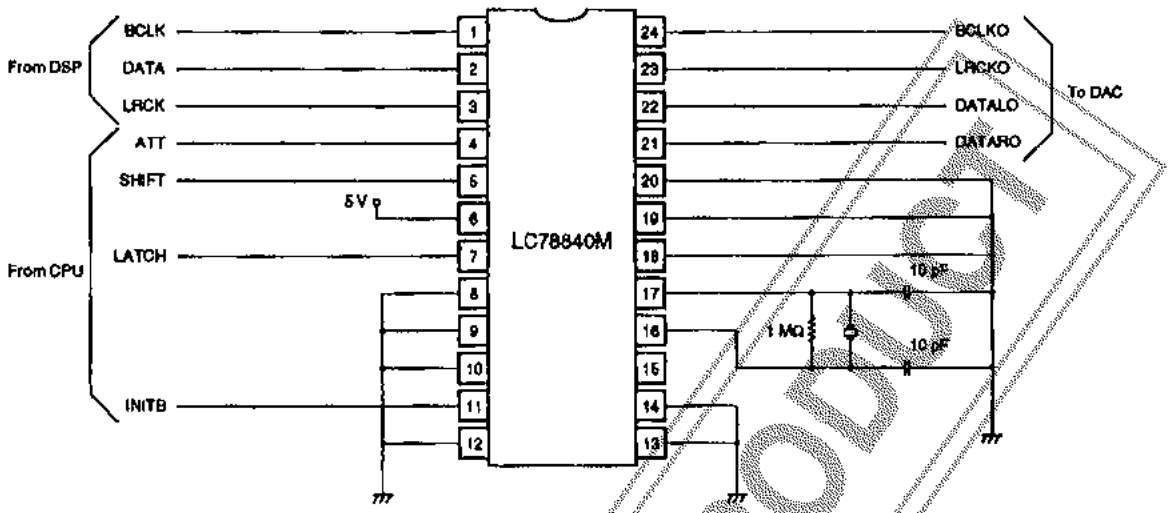


Figure 12. Digital filter