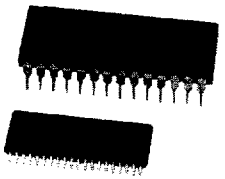
BURR-BROWN®



DF1700

Dual Channel, 8x Oversampling DIGITAL FILTER

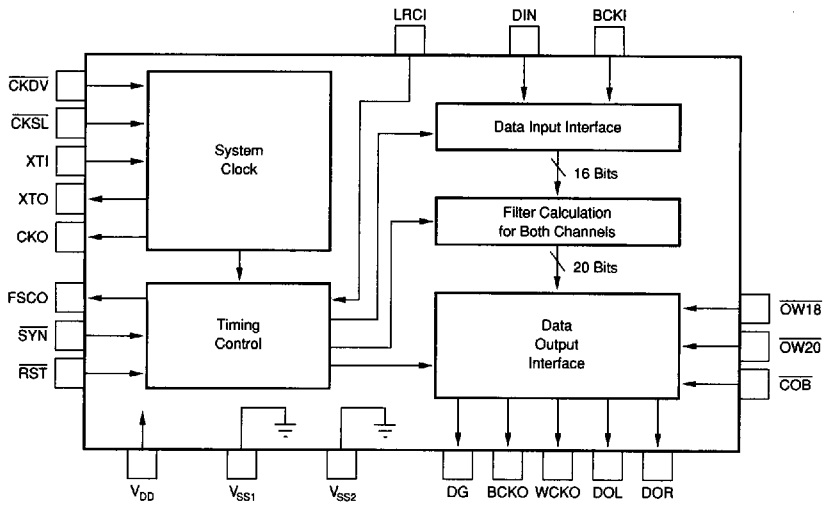
FEATURES

- DUAL CHANNEL DIGITAL INTERPOLATION FILTERS
- ACCEPTS 16-BIT INPUT DATA
- USER-SELECTABLE FOR 16-, 18-, OR 20-BIT OUTPUT DATA
- SERIAL OUTPUT IS COMPATIBLE WITH PCM1700 AND PCM63 DACs
- PASSBAND RIPPLE < 0.00005dB
- STOPBAND ATTENUATION > 110dB
- SINGLE +5V POWER SUPPLY FOR LOW POWER DISSIPATION OF 250mW Max
- PLASTIC 28-PIN DIP AND 40-PIN SOIC PACKAGES

DESCRIPTION

The DF1700 is a high performance, 8x oversampling CMOS digital filter. This filter accepts 16-bit input data and is user-selectable for 16-, 18-, or 20-bit output data. The 8x oversampling feature converts the input data frequency (fs) to an output data frequency of 8 X fs by digital interpolation. By providing 8x oversampled data to an audio DAC, lower order analog filters can be used at the DAC's output, thus reducing filter phase non-linearities. Oversampling with the DF1700 simultaneously improves the fidelity of the analog reconstruction and reduces analog filter complexity at the output of the DAC.

The DF1700 is available in a plastic 28-pin DIP and a 40-pin SOIC package, and is designed for compatibility with the Burr-Brown PCM1700 and PCM63 digital-to-analog converters.



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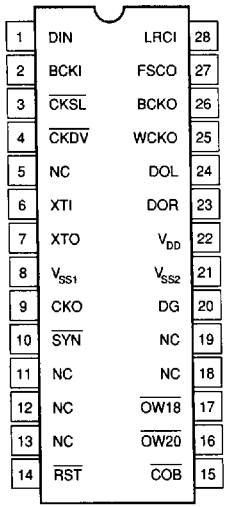
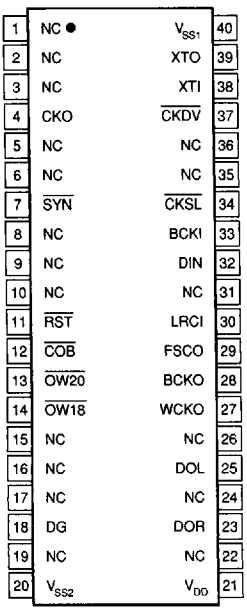
PIN CONFIGURATION

Top View DIP



Top View SOIC



PIN DESCRIPTION

PIN NUMBER SOIC	PIN NUMBER DIP	NAME	I/O[1]	DESCRIPTION
1	–	NC	–	
2	–	NC	–	
3	–	NC	–	
4	9	CKO	O	Clock output (same frequency as XTI input clock).
5	–	NC	–	
6	–	NC	–	
7	10	SYN	I	H: Free-running mode; L: Forced synchronizing mode.
8	11	NC	–	
9	12	NC	–	
10	13	NC	–	
11	14	RST	I	H: Normal operation; L: System reset.
12	15	COB	I	Select output data format— H: Two's complement; L: Complemented offset binary (COB).
13	16	OW20	I	Select number of output data bits.[2]
14	17	OW18	I	Select number of output data bits.[2]
15	–	NC	–	
16	18	NC	–	
17	19	NC	–	
18	20	DG	O	Deglitch control clock.
19	–	NC	–	
20	21	V_{SS2}	–	Ground 2.
21	22	V_{DD}	–	Supply voltage (+5V).
22	–	NC	–	
23	23	DOR	O	Rch serial data output (8fs rate).
24	–	NC	–	
25	24	DOL	O	Lch serial data output (8fs rate).
26	–	NC	–	
27	25	WCKO	O	Output timing control (word clock).
28	26	BCKO	O	Output timing control for serial data (bit clock).
29	27	FSCO	O	Internal timing clock (fs rate)
30	28	LRCI	I	Multiplex clock for Lch/Rch input data (fs rate)—H: Lch; L: Rch.
31	–	NC	–	
32	1	DIN	I	Serial data input.
33	2	BCKI	I	Timing clock for serial input data.
34	3	CKSL	I	Select system clock.[2]
35	–	NC	–	
36	5	NC	–	
37	4	CKDV	I	Select system clock.[2]
38	6	XTI	I	Input for oscillator or external clock (system clock).
39	7	XTO	O	Output for oscillator; not connected when using external clock.
40	8	V_{SS1}	–	Ground 1.

NOTES: (1) I = Input terminal; O = Output terminal. (2) Refer to the Functional Description section for details.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

DC SPECIFICATIONS

ELECTRICAL

DIGITAL CHARACTERISTICS: V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to +70°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	DF1700P, U MIN	DF1700P, U TYP	DF1700P, U MAX	UNITS
INPUT							
Logic Family					CMOS		
Logic Voltages	XTI	V_{IL1}				$0.3V_{DD}$	V
	XTI	V_{IH1}		$0.7V_{DD}$			V
	(1)	V_{IL2}				0.5	V
	(1)	V_{IH2}		2.4			V
Input Leakage Current	XTI	I_{LH}	$V_{IN} = V_{DD}$		10	20	µA
	XTI	I_{LL}	$V_{IN} = 0V$		10	20	µA
	(1)	I_{LH}	$V_{IN} = V_{DD}$			1	µA
Input Current	(1)	I_{IL}	$V_{IN} = 0V$		10	20	µA
OUTPUT							
Logic Family					CMOS		
Logic Voltages	(2)	V_{OL}	I_{OL} = 1.6mA			0.4	V
	(2)	V_{OH}	I_{OH} = –0.4mA	2.5			V
POWER SUPPLY REQUIREMENTS							
Supply Voltages		V_{DD}		4.75	5	5.25	V
Supply Current		I_{DD}	V_{DD} = 5V, F_{SYS} (3)			45	mA
Power Dissipation		P_D	Nominal V_{DD}			250	mW
TEMPERATURE RANGE (Ambient, T_A)							
Specification				–20		70	°C
Operating				–20		70	°C

NOTES: (1) Refers to pins LRCI, DIN, BCKI, $\overline{CKSL}$, $\overline{CKDV}$, $\overline{SYN}$, $\overline{RST}$, $\overline{COB}$, $\overline{OW20}$, and $\overline{OW18}$. (2) Refers to pins CKO, DG, DOL, DOR, WCKO, BCKO, and FSCO. (3) F_{SYS} is the frequency of the internal system clock. $F_{SYS} = F_{XTI}$ with $\overline{CKDV}$ = H and $F_{SYS} = F_{XTI}/2$ with $\overline{CKDV}$ = L.

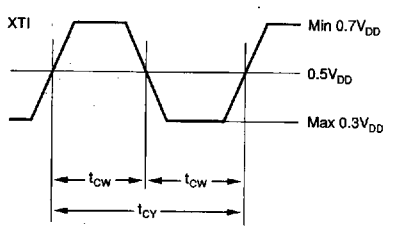
AC SPECIFICATIONS

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to 70°C unless otherwise specified.

PARAMETER	SYMB	CONDITION $\overline{CKSL}$	CONDITION $\overline{CKDV}$	CONDITION x fs(1)	DF1700P, U MIN	DF1700P, U TYP	DF1700P, U MAX	UNITS
CRYSTAL OSCILLATOR								
Oscillating Frequency	f_{MAX}	H	H	192	1		13	MHz
	f_{MAX}	H	L	384	2		26	MHz
	f_{MAX}	L	H	256	1		13	MHz
	f_{MAX}	L	L	512	2		26	MHz
EXTERNAL CLOCK								
Clock Pulse Width	t_{CW}	H	H	192	35		500	ns
	t_{CW}	H	L	384	15		250	ns
	t_{CW}	L	H	256	35		500	ns
	t_{CW}	L	L	512	15		250	ns
Clock Period	t_{CY}	H	H	192	76		1000	ns
	t_{CY}	H	L	384	38		500	ns
	t_{CY}	L	H	256	76		1000	ns
	t_{CY}	L	L	512	38		500	ns

Timing Waveform



NOTES: (1) fs = sampling frequency.

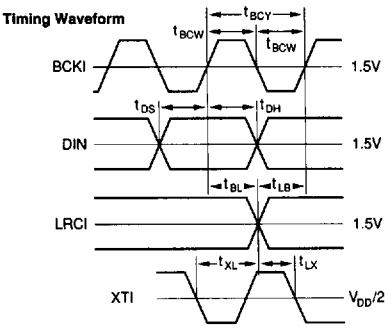
AC SPECIFICATIONS (CONT)

ELECTRICAL

V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = –20°C to 70°C unless otherwise specified.

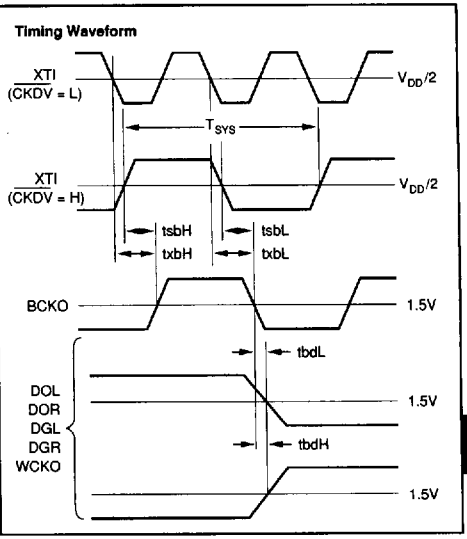
PARAMETER	SYMBOL	DF1700P, U MIN	TYP	MAX	UNITS
INPUT TIMING (BCKI, DIN, LRCI, XTI)					
BCKI, Pulse Width	t_{BCW}	100			ns
BCKI, Cycle Time	t_{BCY}	200			ns
DIN, Setup Time	t_{DS}	75			ns
DIN, Hold Time	t_{DH}	75			ns
Rising Edge of Last BCKI To Edge of LRCI	t_{BL}	75			ns
Edge of LRCI To Rising Edge of First BCKI	t_{LB}	75			ns
Falling Edge of XTI To Rising Edge of LRCI	t_{XL}	20			ns
Rising Edge of LRCI To Falling Edge of XTI	t_{LX}	0			ns

Timing Waveform



PARAMETER	SYMBOL	CONDITION	DF1700P, U MIN	TYP	MAX	UNITS
OUTPUT TIMING						
BCKO Delay Time from XTI	txbH	$\overline{CKDV}$ = L	35		120	ns
	txbL	$\overline{CKDV}$ = L	35		120	ns
	txbH	$\overline{CKDV}$ = H	35		120	ns
	txbL	$\overline{CKDV}$ = H	35		120	ns
Output Delay	tbdL	C_L = 15pF	–10	0	10	ns
	tbdH	C_L = 15pF	–10	0	10	ns

Timing Waveform



ORDERING INFORMATION

DF1700 ( )

- Basic Model Number
- Package Code
  - P: 28-pin Plastic DIP
  - U: 40-pin Plastic SOIC

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DF1700P	28-Pin Plastic DIP	215
DF1700U	40-Pin SOIC	252

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

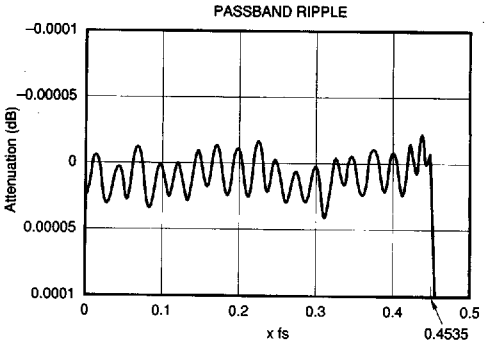
ABSOLUTE MAXIMUM RATINGS

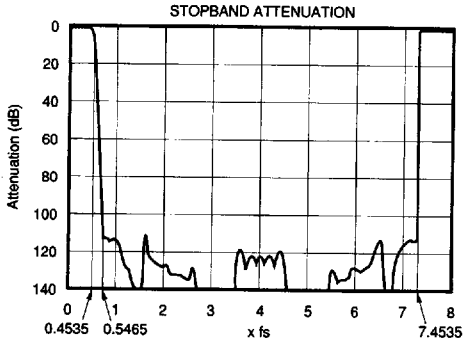
$+V_{DD}$	–0.3V to 7.0V
Input Voltage	–0.3 to V_{DD} +0.3V
Soldering Temperature	255°C
Soldering Time	10s
Storage Temperature	–40°C to +125°C

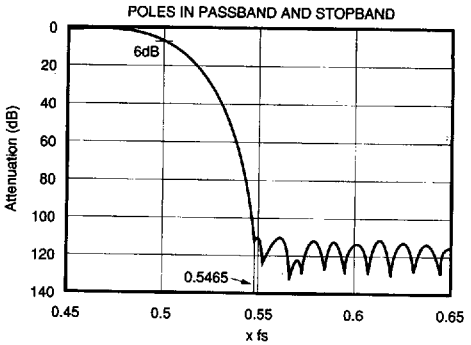
Stresses above these ratings may permanently damage the device.

THEORETICAL FILTER CHARACTERISTICS

PARAMETER	CHARACTERISTICS
Passband	0 ~ 0.4535fs
Stopband	0.5465fs ~ 7.4535fs
Passband Ripple	Within ±0.00005dB
Stopband Attenuation	More than 110dB
Group Delay Time	Constant







THEORY OF OPERATION

The DF1700 has dual filters. Each filter consists of three cascaded, 2x oversampling finite impulse response (FIR) filters as shown in Figure 1. The output of the first, 153-tap filter is again 2x oversampled by the second, 29-tap filter. This 4x oversampled data is again 2x oversampled by a third, 17-tap filter. This oversampling technique further separates the desired analog signal and the sampling frequency. This is desirable because a low-pass filter is required at the output of a DAC to remove all unwanted frequency components caused by the sampling frequency. With the analog signal frequency further separated from the sampling frequency, a lower order analog filter with much better phase characteristics can be used at the output of the DAC without worrying about fold-over noise.

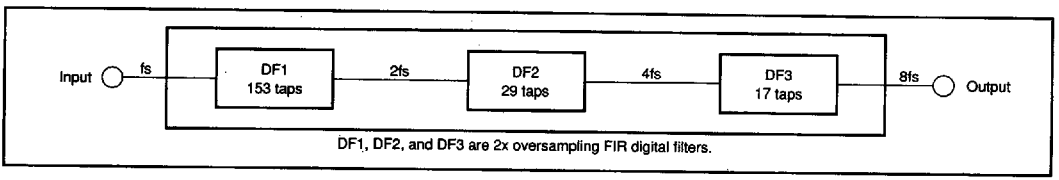


FIGURE 1. Block Diagram of Channel Filter.

FUNCTIONAL DESCRIPTION

SYSTEM CLOCK

The internal system clock of the DF1700 is generated by either a crystal oscillator connected across pins XTI and XTO driving the internal clock generator, or an external clock applied at pin XTI. Four different XTI clock frequencies can be obtained with the control of pins $\overline{\text{CKDV}}$ and $\overline{\text{CKSL}}$. This will provide the correct clock period of the internal system clock as indicated in Table I. For XTI clock frequencies of 384fs and 512fs, the clock is divided by two for internal use. The system clock signal of the same frequency as pin XTI is available at pin CKO.

DATA

Serial Data Input

The 16-bit input data format is two's complement and MSB first. The serial data input timing is the rising edge of BCKI (Figure 2). Consequently the input serial data must be changed at the falling edge of BCKI. The input data is latched to the internal register at the edge of LRCI.

Serial Data Output

The serial data output mode is selected by pins $\overline{OW18}$ and $\overline{OW20}$ as shown in Table II.

The output data format is MSB first and either two's complement or complementary offset binary (COB). The format of output data is selected by the $\overline{COB}$ pin:

$\overline{COB}$ = H Two's complement
$\overline{COB}$ = L Complemented Offset Binary (COB)

The output data from the DF1700 can be fed directly to the data inputs of either the PCM1700 or PCM63 with the BCKO clock output serving as the input clock to these DACs. The data bits will be clocked into the DAC on the rising edges of BCKO (Figure 3).

CONDITION		XTI CLOCK (F_{XI})	CLOCK PERIOD OF INTERNAL SYSTEM CLOCK
$\overline{CKDV}$	$\overline{CKSL}$		
H	H	192fs	$1/F_{XI}$
H	L	256fs	$1/F_{XI}$
L	H	384fs	$2/F_{XI}$
L	L	512fs	$2/F_{XI}$

NOTE: fs = sampling frequency.

TABLE I. System Clock Frequency Selection.

$\overline{OW18}$	$\overline{OW20}$	NO. OF OUTPUT DATA BITS
H	H	16
L	H	18
H	L	20

TABLE II. Programming the Number of Output Data Bits.

CLOCK SYNCHRONIZATION

The internal clock for the arithmetic circuitry and output interface is derived by the system clock from the XTI pin, and is independent of the input circuitry timing from the BCKI and LRCI input clocks. There are two synchronization modes: the Free-Running Mode and the Forced Synchronization Mode.

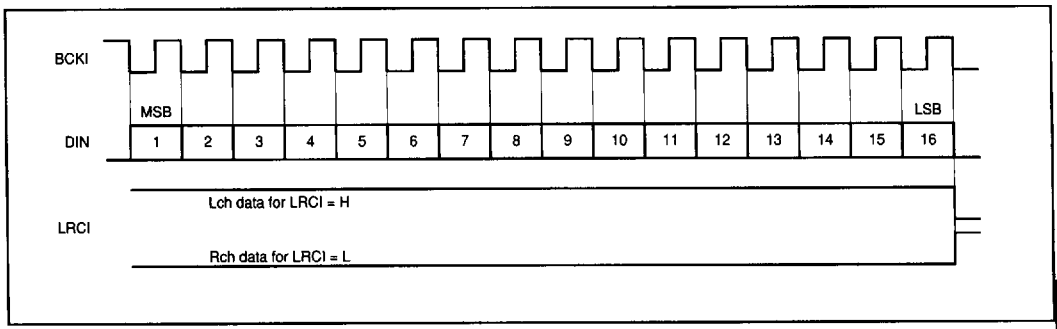


FIGURE 2. Input Timing Waveforms for Clocking Data into the DF1700.

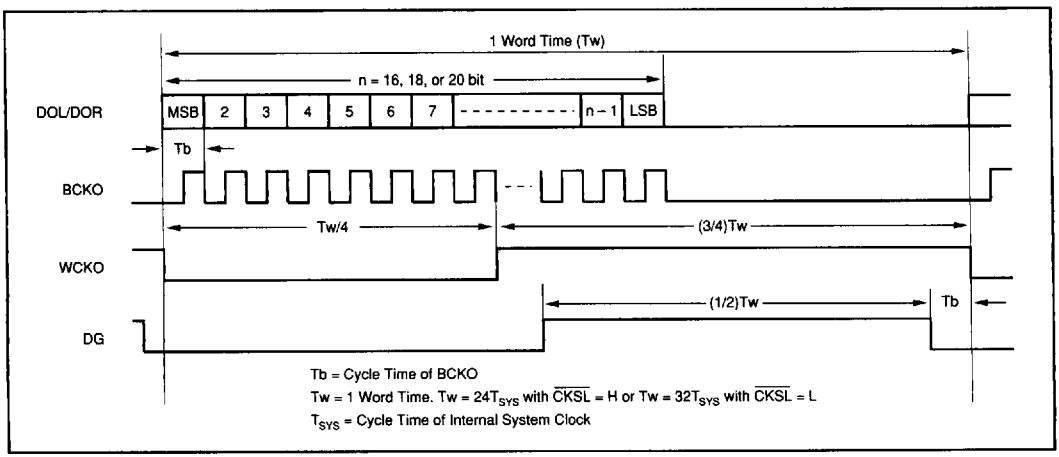


FIGURE 3. Output Data Timing Waveforms.

Free-Running Mode ($\overline{SYN}$ = H)

No adjustment of the internal clock takes place for phase differences between the internal clock and the LRCI clock of up to ±3/8 of the input data sample period (1/fs). Hence, internal timing is not affected even if jitter is present on the LRCI clock input, and no jitter or timing glitches appear on the data output. If the clock phase differences exceed the ±3/8fs limit, or if the RESET function is executed, the internal clock is synchronized to the rising edge of LRCI.

Forced Synchronization Mode ($\overline{SYN}$ = L)

In this mode the internal clock is resynchronized at each rising edge of LRCI. Note that device misoperation may occur if jitter in the LRCI input shortens the LRCI period below the required system clock period. Furthermore, if the LRCI period is too long, internal arithmetic operations will function correctly, but output timing is adversely affected.

The internal timing clock derived from the system clock is available at the FSCO pin.

SYSTEM RESET

The RESET function is useful for synchronizing the internal arithmetic circuitry and output section clock with the LRCI external input clock when operating in the free-running mode ($\overline{SYN}$ = H). It is not necessary to reset in the forced synchronization mode. Reset is also not required if the output timing needs not be synchronized with LRCI. Figure 4 shows the connection to reset the DF1700 on power-up.

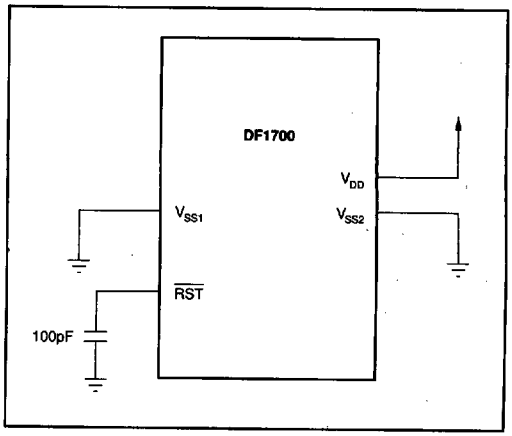
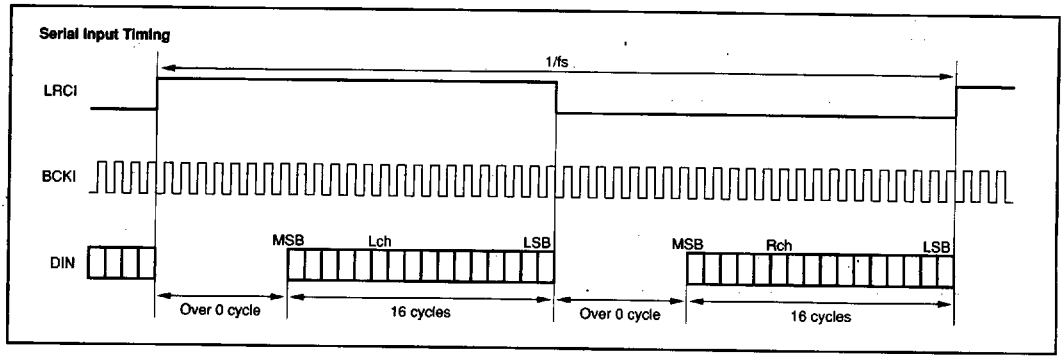
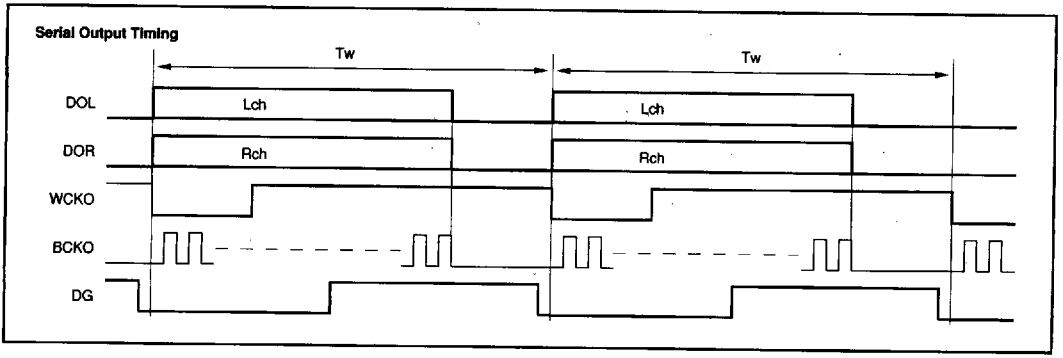


FIGURE 4. System Reset Circuit.

TIMING DIAGRAMS





APPLICATIONS

The most common application for the DF1700 is in high performance digital audio playback such as compact disc players. Digital information from a compact disc is often formatted using a digital interface format receiver chip (DIFRC). The DF1700 can be interfaced directly to the output of many popular DIFRCs as shown in Figure 5.

The fs data stream which has been formatted by the DIFRC is 8x oversampled by the DF1700 and separated into left and right channel data for input to the PCM1700 DAC (Figure 6). The analog stereo outputs from the PCM1700 each pass through a three pole Generalized Immittance Converter (GIC) low-pass filter which has extremely low distortion and negligible phase shift. An evaluation board, the DEM1143, is available from Burr-Brown for the PCM1700/DF1700. This board has the features mentioned above as well as an AES/EBU interface and breadboard area for user experimentation. Figure 7 shows a similar circuit diagram with the DF1700 providing 8x oversampled data to a pair of PCM63 DACs.

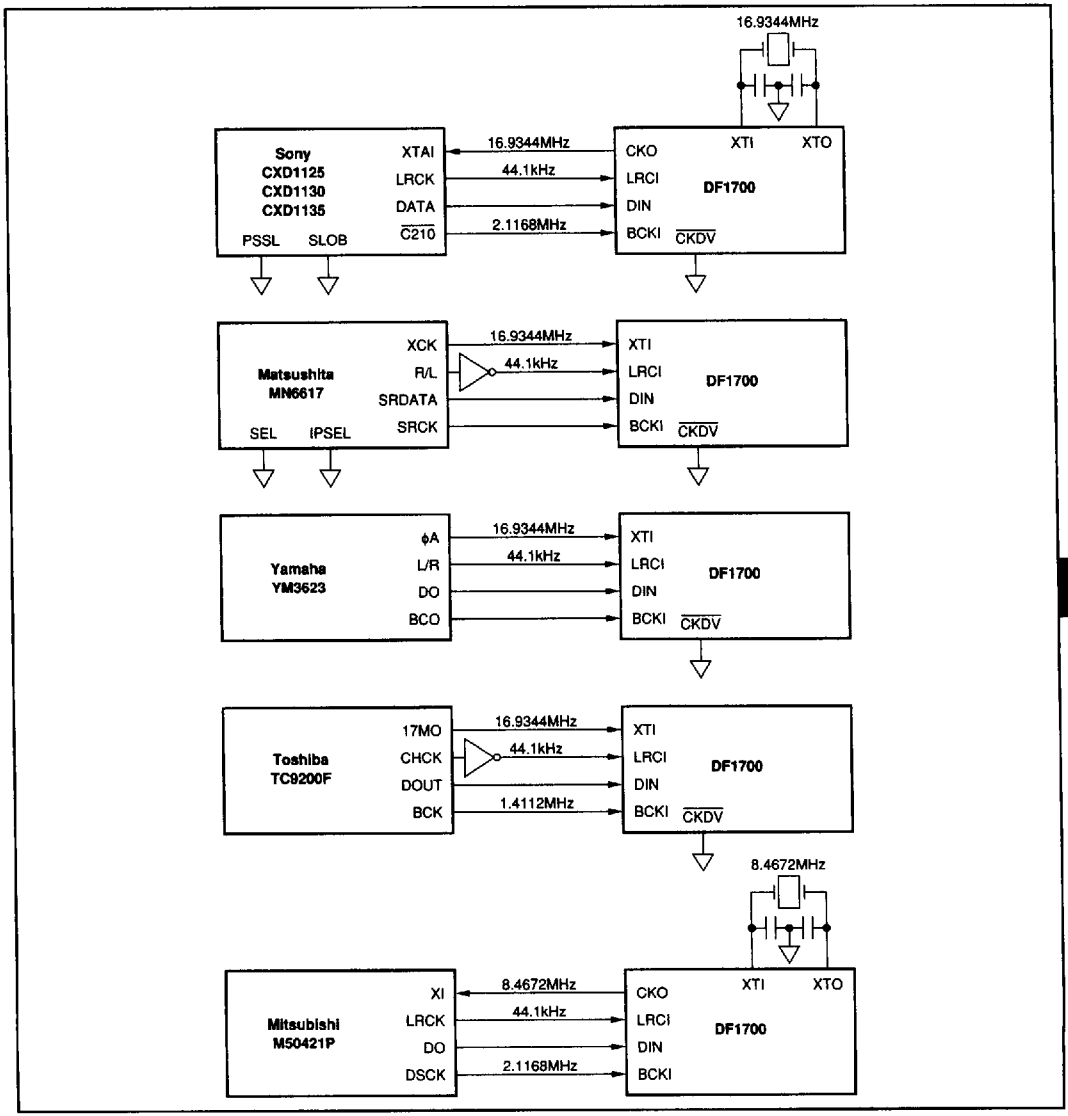


FIGURE 5. Interfacing the DF1700 to Various Digital Interface Format Receiver Chips (DIFRCs).

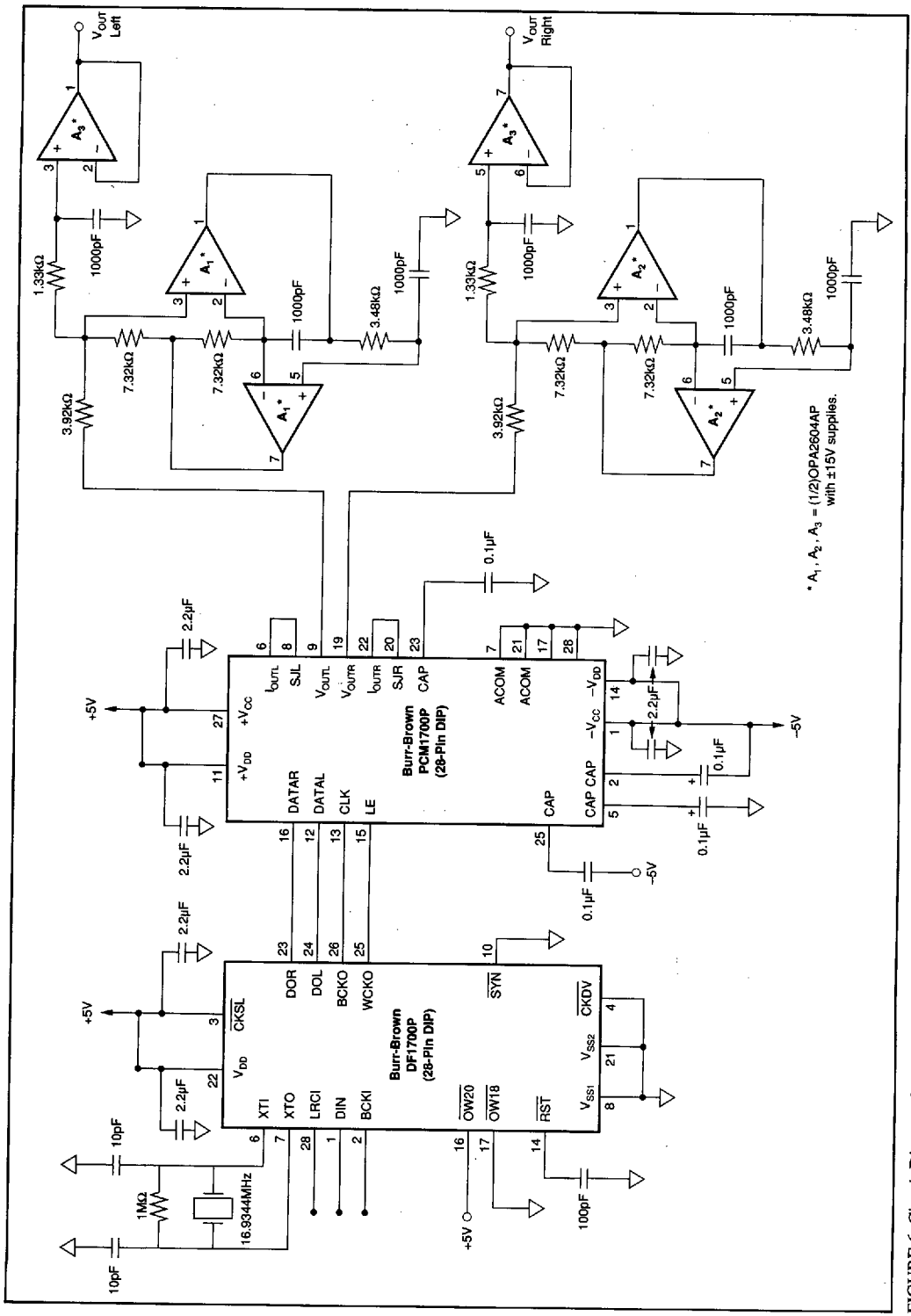


FIGURE 6. Circuit Diagram for the DF1700 Providing Oversampled Data to the PCM1700P Dual-Channel DAC.

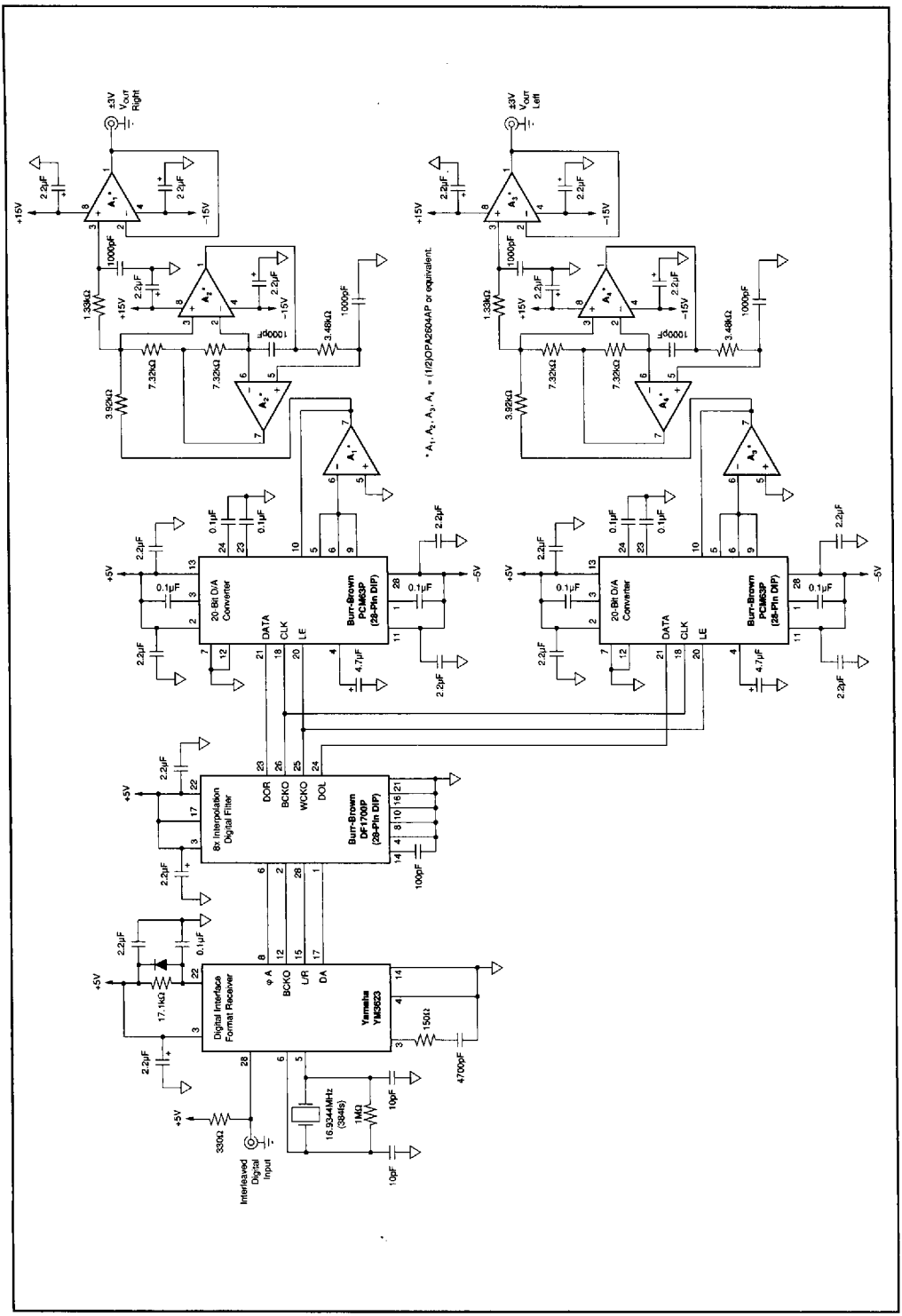


FIGURE 7. Circuit Diagram for the DF1700 Providing Oversampled Data to a Pair of PCM63P DACs.