



## Pin Description

Pin No.	Symbol	I/O	Description
1	V <sub>DD2</sub>	—	Analog power supply
2	V <sub>SS</sub>	—	Analog GND
3	R (-)	O	Rch PLM output (Opposite phase)
4	V <sub>DD</sub>	—	Analog power supply
5	V <sub>SS2</sub>	—	Analog GND
6	V <sub>SUB</sub>	—	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV <sub>DD</sub>	—	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin. Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V <sub>SUB</sub>	—	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DV <sub>SS</sub>	—	Digital GND
28	V <sub>SUB</sub>	—	Sub straight. Connect to GND.
29	V <sub>SS2</sub>	—	Analog GND
30	V <sub>DD</sub>	—	Analog power supply
31	L (-)	O	Lch PLM output (Opposite phase)
32	V <sub>SS</sub>	—	Analog GND
33	V <sub>DD2</sub>	—	Analog power supply
34	V <sub>SS</sub>	—	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V <sub>DD</sub>	—	Analog power supply
37	V <sub>SUB</sub>	—	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	—	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XVDD	—	Clock power supply
42	VDD	—	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	VSS	—	Analog GND

## Electrical Characteristics

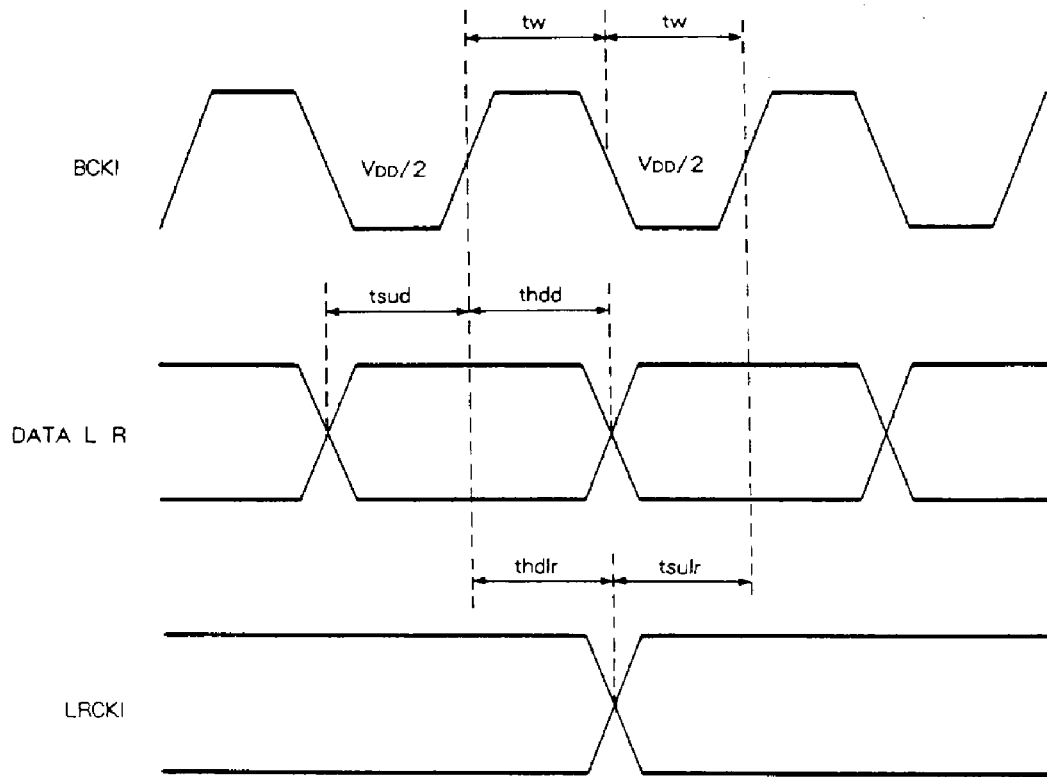
### DC Characteristics (VDD=VDD2=DVDD=XVDD=5.0V ± 5%, VSS=VSS2=DVSS=XVSS=0V, Topr=-10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V <sub>IH</sub>	—	0.76V <sub>DD</sub>			V
"L" input voltage	V <sub>IL</sub>	—			0.24V <sub>DD</sub>	V
Input leak current	I <sub>II</sub>	—			± 5.0	μA
"H" output voltage (DINIT, INAF)	V <sub>OH</sub>	I <sub>o</sub> =-1mA	V <sub>DD</sub> -0.5			V
"L" output voltage (DINIT, INAF)	V <sub>OL</sub>	I <sub>o</sub> =1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V <sub>OH</sub>	I <sub>o</sub> =-0.4mA	V <sub>DD</sub> -0.5			V
"L" output voltage(512Fs, LRCKO)	V <sub>OL</sub>	I <sub>o</sub> =0.4mA			0.4	V
"H" output voltage (128Fs)	V <sub>OH</sub>	I <sub>o</sub> =-0.3mA	V <sub>DD</sub> -0.5			V
"L" output voltage (128Fs)	V <sub>OL</sub>	I <sub>o</sub> =0.3mA			0.4	V
"H" output voltage (R+, R-, L+, L-)	V <sub>OH</sub>	I <sub>o</sub> =-15mA	V <sub>DD</sub> -0.5			V
"L" output voltage (R+, R-, L+, L-)	V <sub>OL</sub>	I <sub>o</sub> =15mA			0.5	V
"H" output voltage (XOUT)	V <sub>OH</sub>	I <sub>o</sub> =-2.0mA	V <sub>DD</sub> -0.5			V
"L" output voltage (XOUT)	V <sub>OL</sub>	I <sub>o</sub> =2.0mA			0.4	V
Current consumption	I <sub>DD</sub>	—		55	80	mA

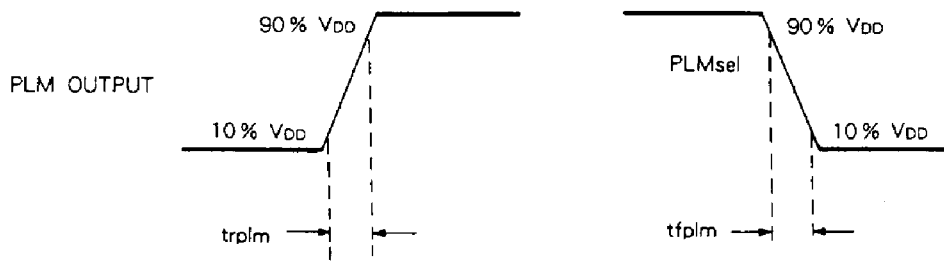
### AC Characteristics (VDD=VDD2=DVDD=XVDD=5.0V ± 5%, VSS=VSS2=DVSS=XVSS=0V, Topr=-10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	t <sub>w</sub>		38			nsec
DATAL, R set up time	t <sub>suD</sub>		18			nsec
DATAL, R hold time	t <sub>hDd</sub>		18			nsec
LRCKI set up time	t <sub>suLr</sub>		18			nsec
LRCKI hold time	t <sub>hLr</sub>		18			nsec
PLM output rise/fall time	t <sub>r</sub> , t <sub>f</sub>	CL=300pF		10		nsec

• Input



• Output



**Analog Characteristics** ( $V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V$ ,  $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$ ,  $T_a=25^\circ C$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data ( $F_s=44.1kHz$ )			0.0030	%
S/N ratio	S/N	1kHz, 0dB/ $-\infty$ dB data ( $F_s=44.1kHz$ ) (A filter used)	96			dB

**Electrical Characteristics Testing Method**

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

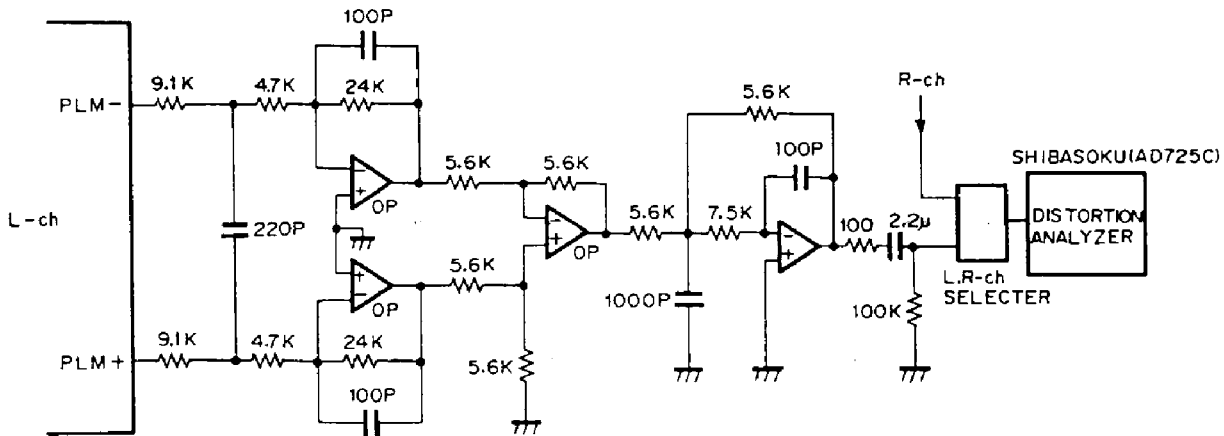


Fig. 1.

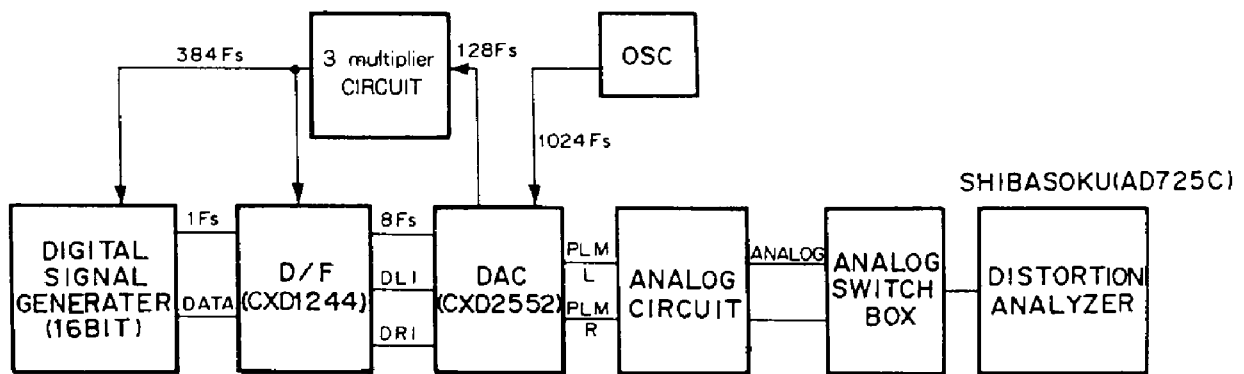


Fig. 2.

**Description of Function**

**I/O Synchronizing Circuit**

1) Theory of operation

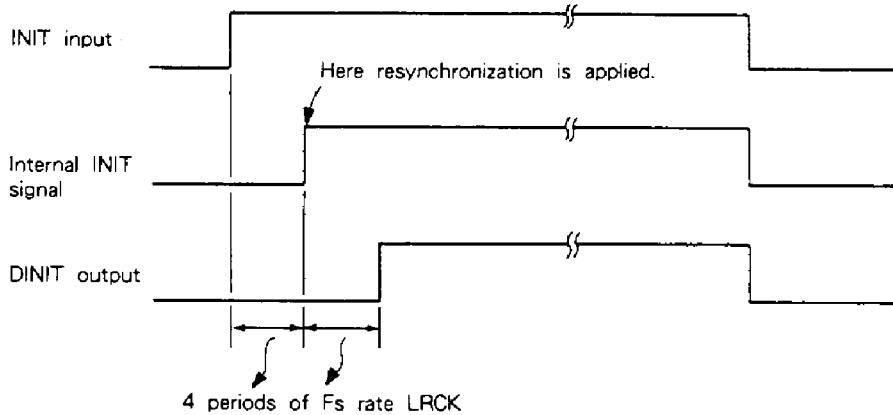
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK<sub>F</sub>) of the LRCK input has entered the window or not.

When power supply is turned on, should LRCK<sub>F</sub> be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK<sub>F</sub>. Synchronization between the exterior system and this LSI is established through this operation.

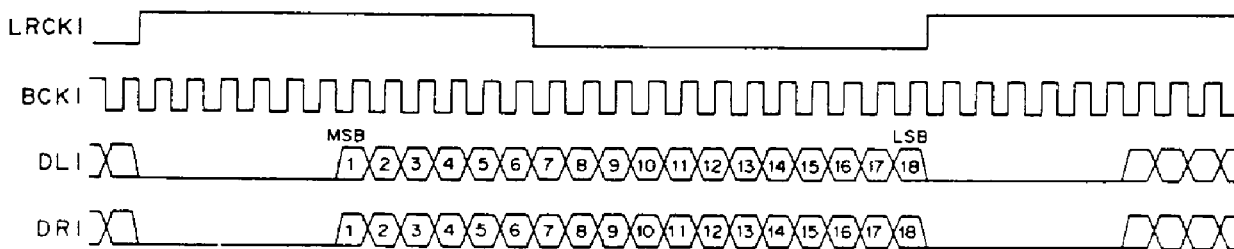
2) Resynchronization by means of INIT

Even when LRCK<sub>F</sub> is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK<sub>F</sub> is located at the center of the window.

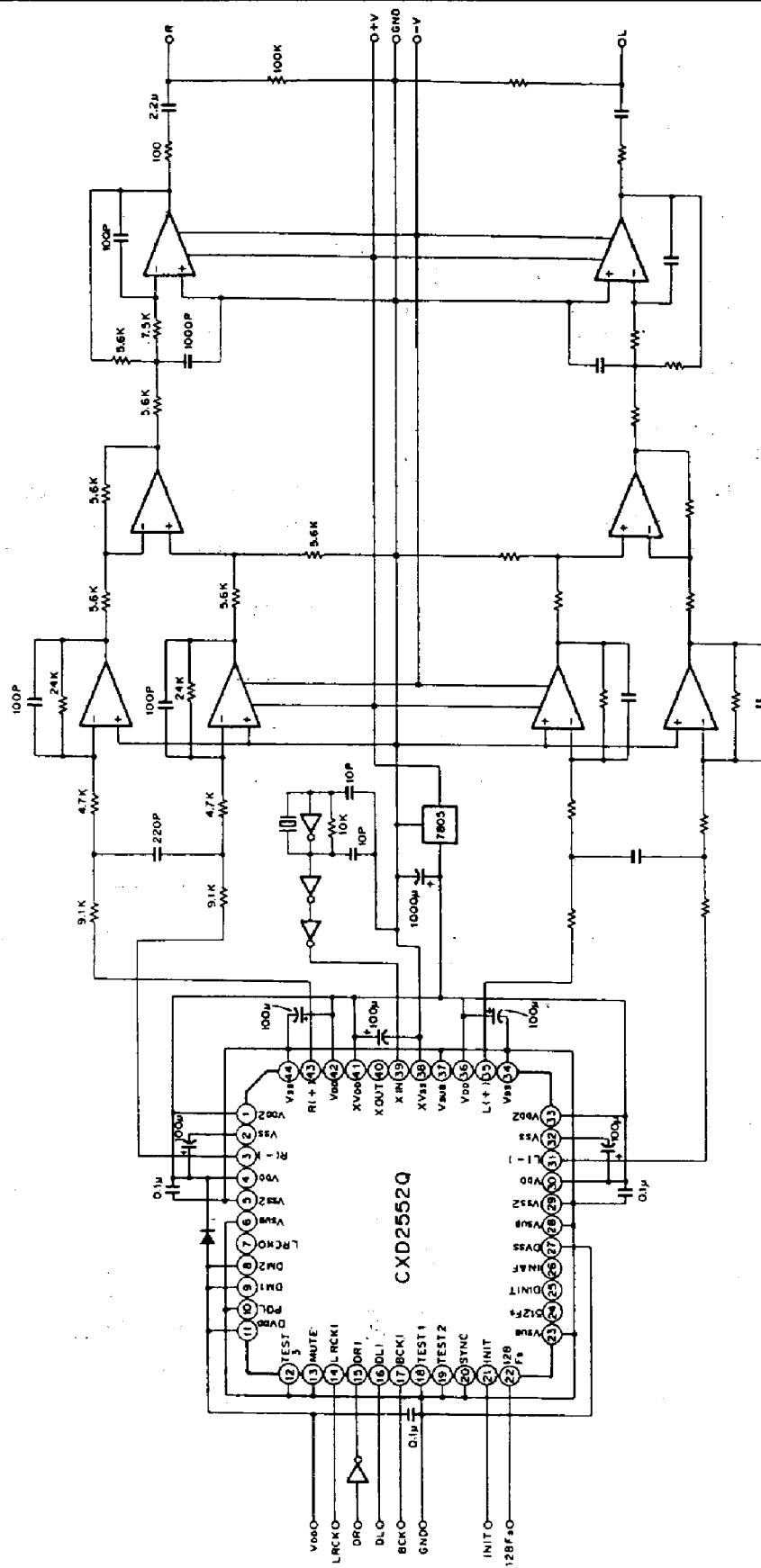
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.



**Input Timing (8fs rate)**

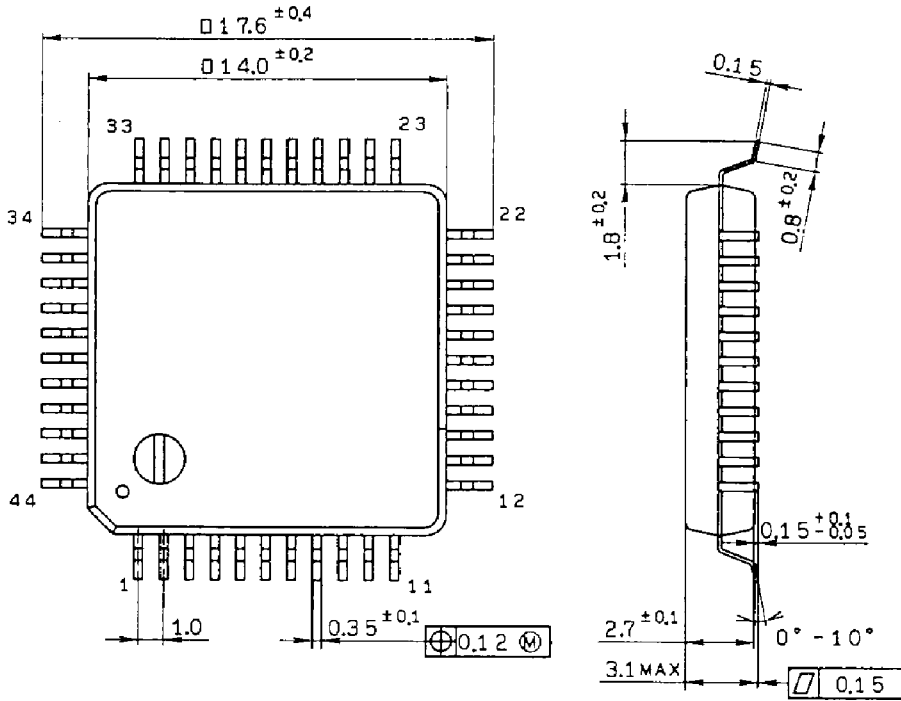


Application Circuit



Package Outline Unit : mm

44pin GFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	_____