SONY

CX23034

Digital Filter for CD

Description

The CX23034 is a silicon gate CMOS LSI which has been developed as a digital filter for compact disc player. Excellent filter characteristics can easily be realized by inserting CX23034 between digital signal processing LSI CX23035 for CD and D/A converter.

Features

- Composition of filter:
  - Stereo signal processing with 1 chip
  - Two times sampling rate conversion
  - FIR filter with 16-bit coefficient
  - Filter length 96
- Characteristics of filter:
  - Linear phase
  - Band passing ripple lower than +0.01 dB
  - Stopband attenuation higher than 80 dB
  - Frequency characteristics designed to correct the aperture effect of D/A converter
- Overflow limiter
- Formmats of the output data can be selected either to two's complement or offset binary
- Interface possible with 16-bit serial input D/A converter
- Use together with CX23035 in pair

Structure

Silicon gate CMOS

Absolute Maximum Ratings (Ta=25°C)

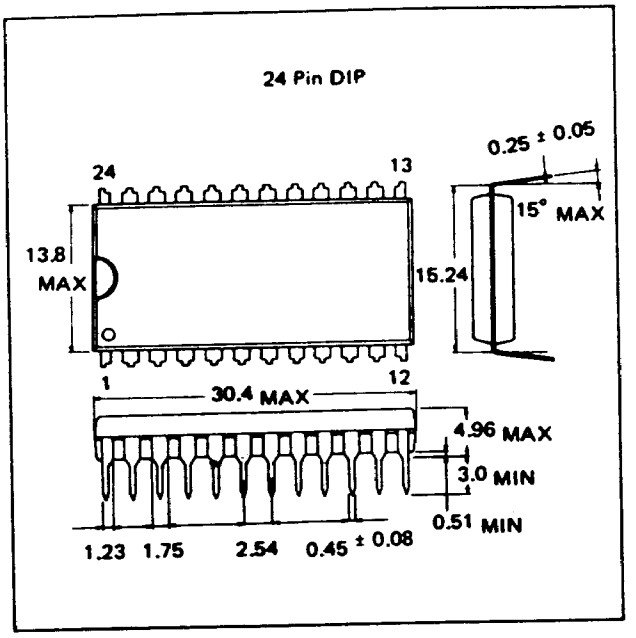
• Power supply voltage	V_{DD}	V_{SS}*	−0.3 to +7.0	V
• Input voltage	V_{IN}	V_{SS}*	−0.3 to +7.0	V
• Output voltage	V_{OUT}	V_{SS}*	−0.3 to +7.0	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

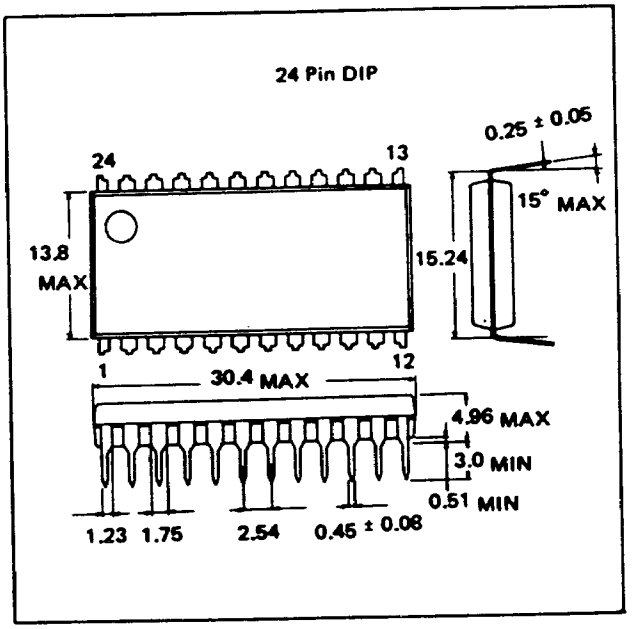
* V_{SS} = 0V

Recommended Operating Conditions

• Power supply voltage	V_{DD}		4.5 to 5.5	V
• Input voltage	V_{IN}	V_{SS}	−0.3 to V_{DD} +0.3	V
• Operating temperature	Topr		−20 to +75	°C

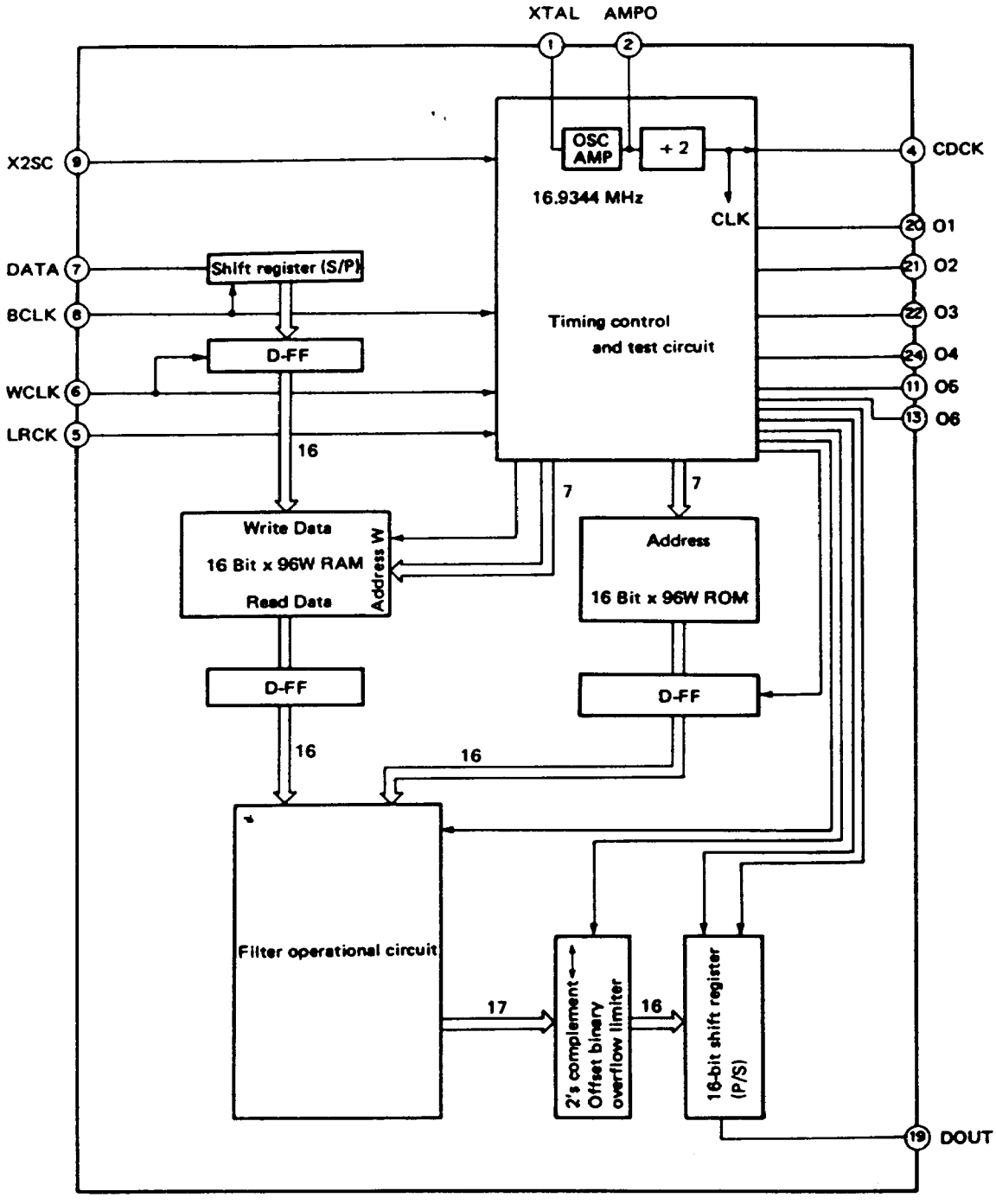
Package Outline Unit: mm



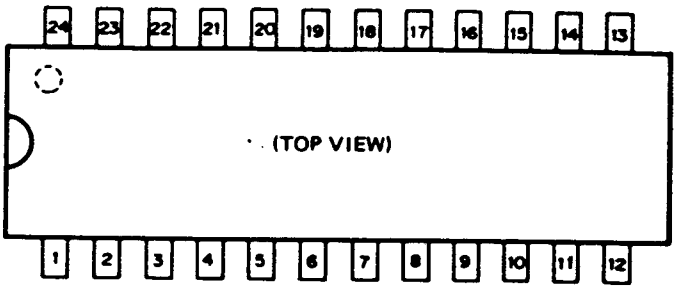


50293-ST

Block diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	XTAL	I	Input for crystal oscillator (16.9344 MHz)
2	AMPO	O	Output for crystal oscillator (16.9344 MHz)
3	TSET1	I	Input for testing (Normally connected to Vss)
4	CDCK	O	Clock output (8.4672 MHz)
5	LRCK	I	44.1 kHz strobe input
6	WCLK	I	88.2 kHz strobe input
7	DATA	I	Serial data input (Two's complement, MSB first)
8	BCLK	I	Bit clock input (input for serial data)
9	X2SC	I	Input for output format selection (High offset binary, low two's complement)
10	TEST2	I	Input for test (normally connected to Vss)
11	O5	O	Timing signal
12	Vss	—	GND pin (0V)
13	O6	O	Timing signal
14	TEST3	O	Test data output (normally open)
15	TEST4	O	Test data output (normally open)
16	TEST5	O	Test data output (normally open)
17	TEST6	O	Test data output (normally open)
18	TEST7	O	Test data output (normally open)
19	DOUT	O	Serial data output (MSB first)
20	O1	O	Timing signal
21	O2	O	Timing signal
22	O3	O	Timing signal
23	O4	O	Timing signal
24	V_{DD}	—	Power supply pin (+5V)

Note) The frequencies shown are values to be used for CD.

Input/Output Capacity

Item	Symbol	Standard			Unit
		Min.	Typ.	Max.	
Input pin	C_{IN}		8	12	pF
Output pin	C_{OUT}		10	12	pF

Measuring condition: V_{DD}=V_{IN}=0V, FM=1 MHz

Electrical Characteristics

DC characteristics

V_{DD}=5V±10%, V_{SS}=0V, Topr=−20 to +75°C

Item		Symbol	Condition	Standard			Unit
				Min.	Typ.	Max.	
Supply current		I_{DD}	V_{DD}=5.0V		35		mA
		I_{DDS}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=V_{SS}			0.1	mA
Input voltage (1) H level	A group (note)	V_{IH1}		0.7V_{DD}			V
Input voltage (1) L level		V_{IL1}				0.3V_{DD}	V
Input voltage (2) H level	B group (note)	V_{IH2}		2.2			V
Input voltage (2) L level		V_{IL2}				0.8	V
Output voltage H level	C group (note)	V_{OH}	I_{OH}=1 mA	V_{DD}−0.5		V_{DD}	V
Output voltage L level		V_{OL}	I_{OL}=1 mA	0		0.4	V
Input leakage current	B group (note)	I_{LI}		−5		5	uA

Note) Pins of from A to C groups are shown as below.

A group	XTAL
B group	TEST1, TEST2, X2SC, DATA, BCLK, WCLK, LRCK
C group	CDCK, O1, O2, O3, O4, O5, O6, DOUT, TEST3, TEST4, TEST5, TEST6, TEST7

AC Characteristics

Input AC characteristics Topr=−20 to +75°C, V_{DD}=5V±10%

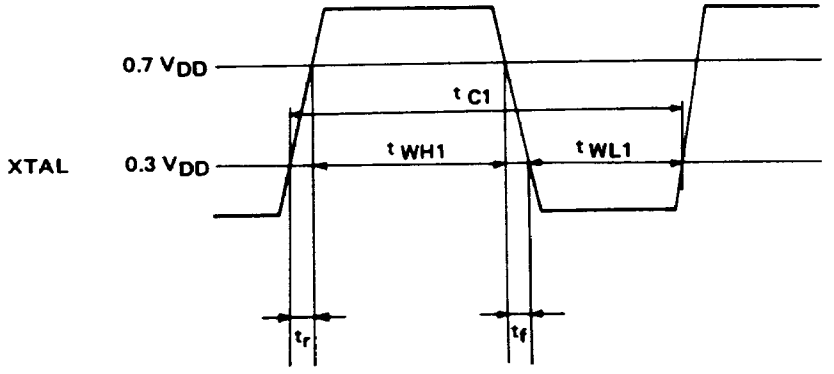
(1) XTAL pin

① In the event crystal oscillator is used

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillating frequency	f_{MAX}	· .		18.432	MHz

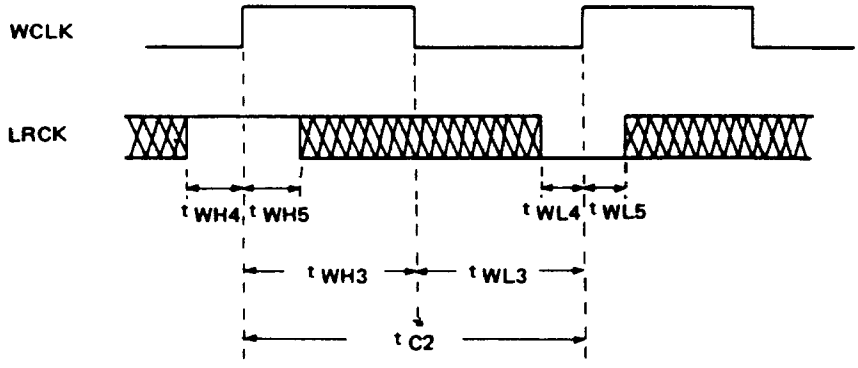
② In the event pulse is input while crystal oscillator is not being used

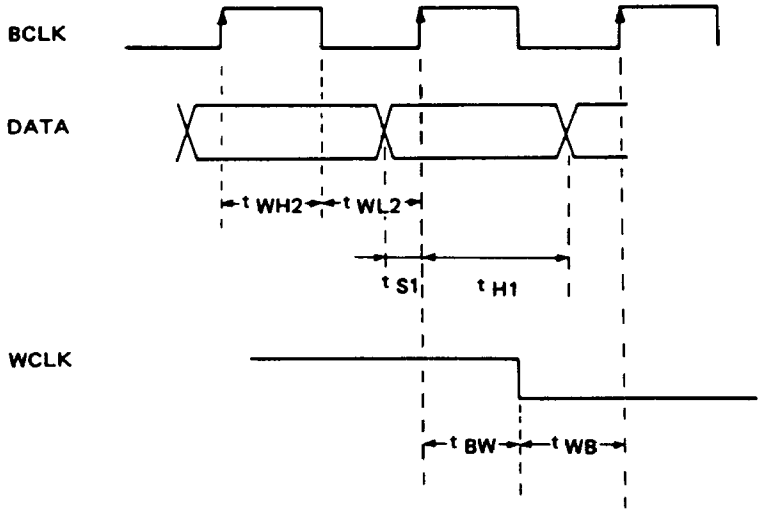
Item	Symbol	Min.	Typ.	Max.	Unit
Pulse cycle	t_{C1}	54	59		ns
"H" level pulse width	t_{WH1}	12	19.5		ns
"L" level pulse width	t_{WL1}	12	19.5		ns
Rising time	t_r		10	15	ns
Falling time	t_f		10	15	ns



(2) DATA, BCLK, WCLK and LRCK pins

Item	Symbol	Min.	Typ.	Max.	Unit
BCLK "H" level pulse width	t_{WH2}	59			ns
BCLK "L" pulse level width	t_{WL2}	48			ns
DATA hotting-up time	t_{S1}	13			ns
DATA holding time	t_{H1}	59			ns
WCLK "H" level pulse width	t_{WH3}	3543		7795	ns
WCLK "L"level pulse width	t_{WL3}	3543		7795	ns
WCLK pulse cycle	t_{C2}		11338		ns
From rising of BCLK to falling of WCLK	t_{BW}	65			ns
From falling of WCLK to rising of BCLK	t_{WB}	22			ns
LRCK "H" level pulse width 1	t_{WH4}	0			ns
LRCK "H" level pulse width 2	t_{WH5}	473			ns
LRCK "L" level pulse width 1	t_{WL4}	0			ns
LRCK "L" level pulse width 2	t_{WL5}	473			ns





Function Explanation

(1) Oscillation circuit

Connect a crystal oscillator with a oscillation frequency of 384 fs (16.9344 MHz) between XTAL pin and AMPO pin, as shown in Fig. 1. In the event crystal oscillation is not used, input clock signal with a frequency of 384 fs to the XTAL pin.

The clock signal of 192fs (8.4672 MHz), which is divided-by 2 of the crystal oscillation frequency, is output from the CDCK pin.

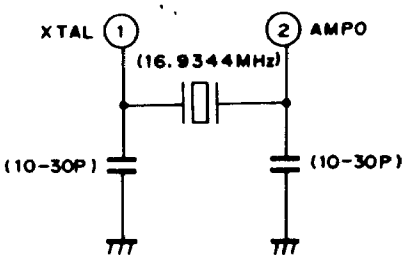


Fig. 1 Oscillation circuit

[The values shown in parentheses are those used for CD]

(2) Regarding initialization

The initialization of this LSI requires a XTAL time of approx. 770 clocks after the power supply is turned on, provided that all inputs are in normal condition. (It takes approx. 46 μs when XTAL 16.9344 MHz.) The output is not valid until the initialization is completed.

(3) Interface with signal processing LSI

Interfacing with the signal processing LSI can be carried out as shown in Fig. 2.

The input data 16 bit (two's complement) is input to DATA pin with MSB first, and individual bits of DATA input are fetched into the shift register within the IC at rising of BCLK. Accordingly, individual bits of DATA input should be changed at the falling of BCLK. Thus, 16 bits of data in the shift register within the LSI at the falling of WCLK is latched as a writting data of RAM.

Therefore, BCLK signal requires at least 16 pulses during its falling time of WCLK to the next falling time of same. If the BCLK signal has 17 pulses or over during its falling time of WCLK to the next falling time of same, 16 bits before WCLK falling time become writting data of RAM.

The input data becomes L-ch signal when LRCK is "H", and R-ch signal when LRCK is "L".

(4) Interface with D/A converter

It enables to be interfaced with various D/A converter by using X2SC pin. The output timing chart is as shown in Fig. 2.

X2SC (Switchover of offset binary two's complement)

X2SC = "H" offset binary

X2SC = "L" two's complement

Offset binary is MSB inverse of two's complement.

(5) Regarding synchronizing with input and output signals

If the relative relation between rising of WCLK when LRCK is "L" and output signal differs by more than 2 clocks of CDCK (236 ns), the operation within the IC is momentarily stopped, and synchronization of input signal and output signal is performed again.

(6) Regarding frequency characteristics of filter

The frequency characteristics of this LSI are as shown in Figs. 3 and 4.

(7) Correction of aperture effect frequency characteristics of D/A converter

The digital output of this LSI is output after correcting the frequency characteristics against the aperture effect of the D/A converter. In addition, this correction is carried out on the assumption that the sample and hold type DEGRETCHER is used as an analog output of the D/A converter.

Timing Chart

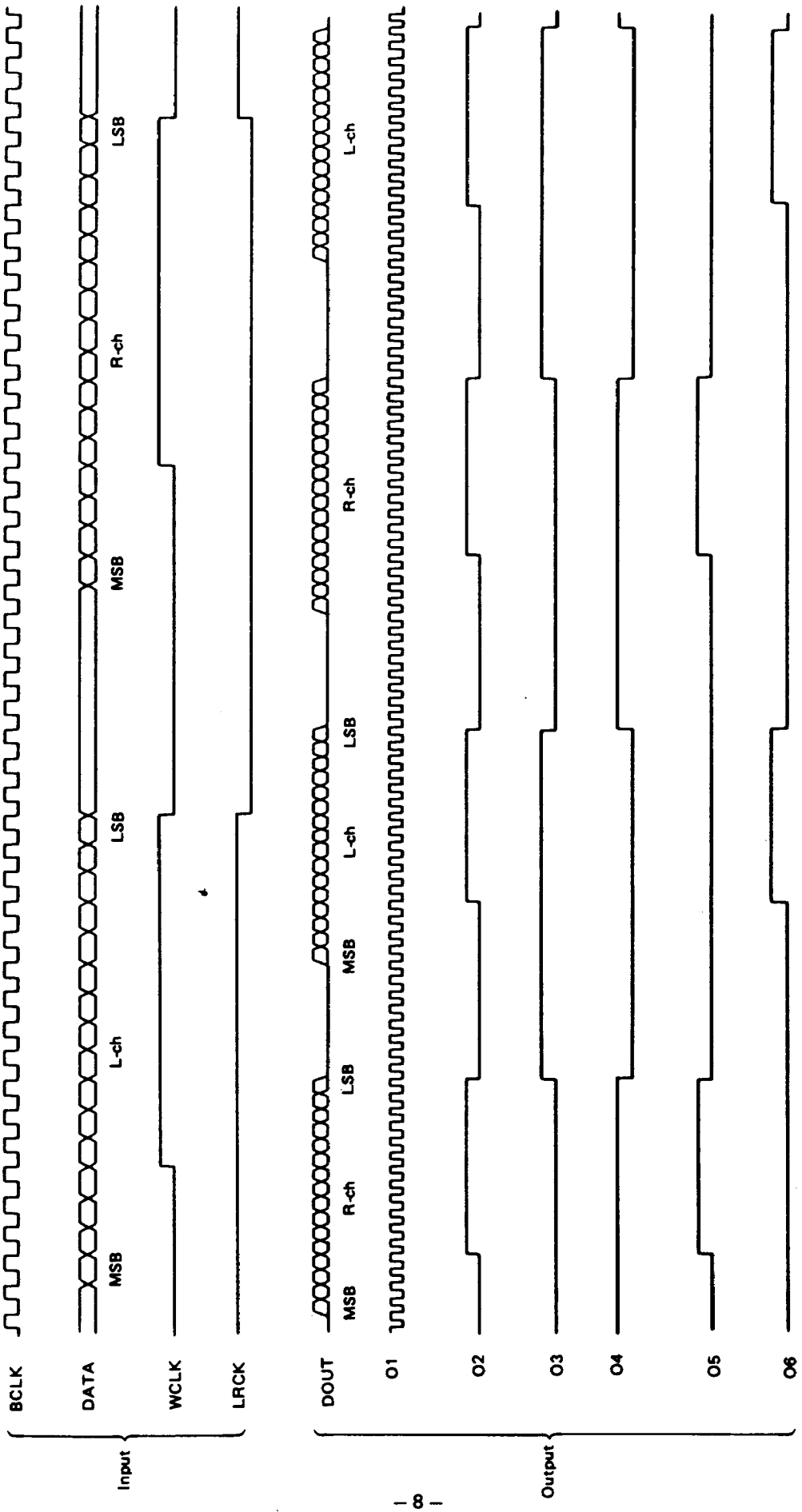


Fig. 2 CX23034 timing chart

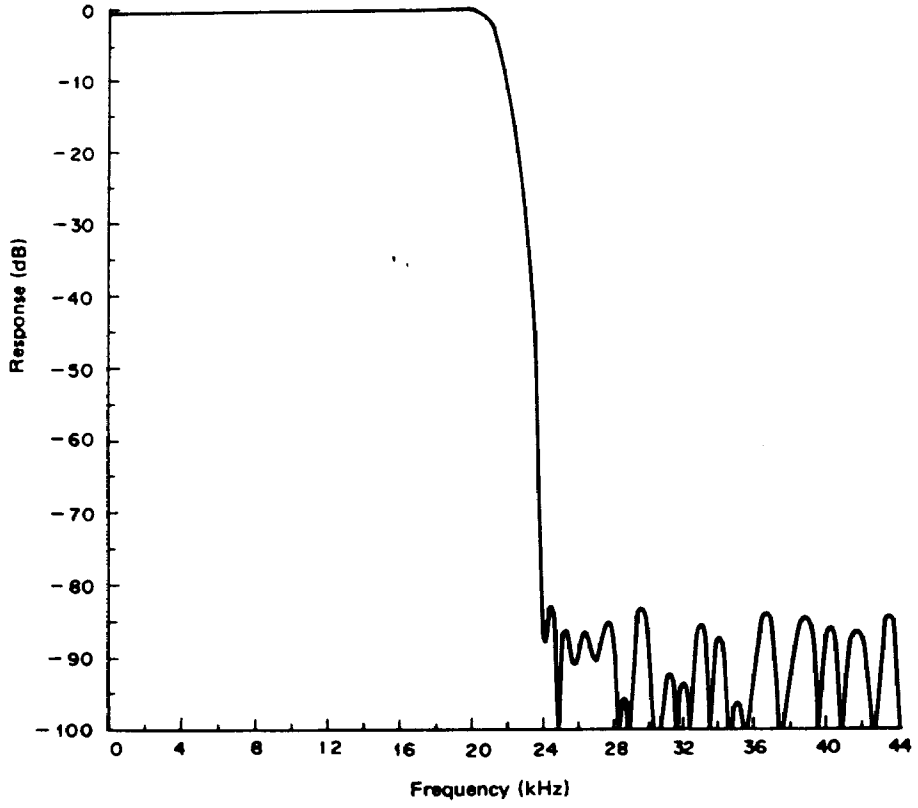


Fig. 3 Frequency characteristics

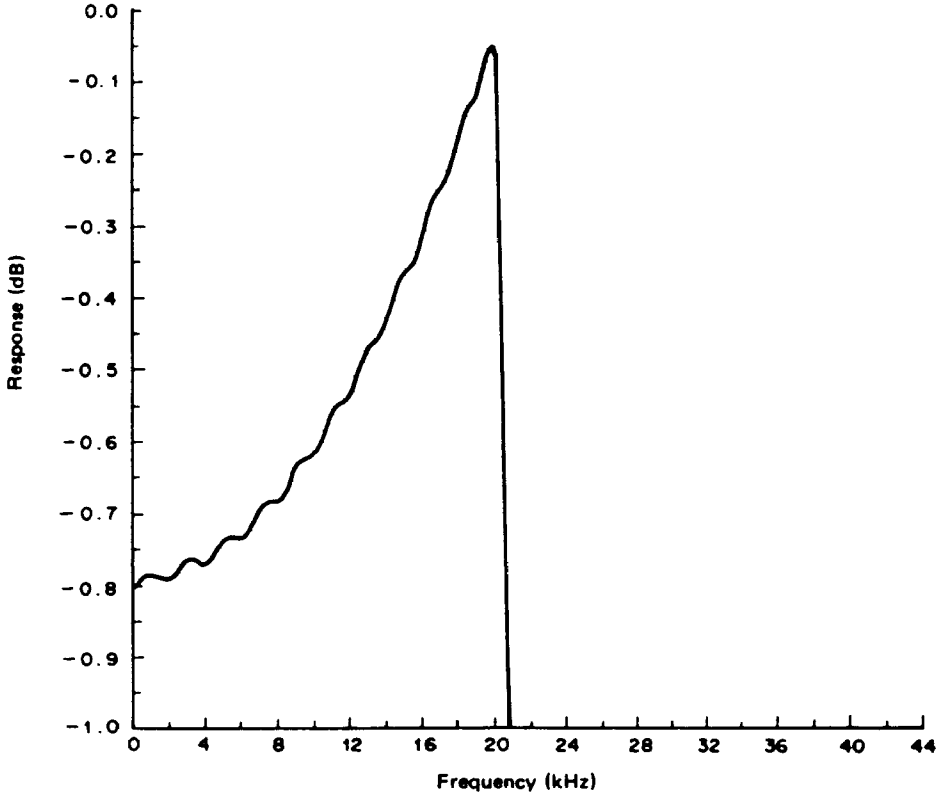
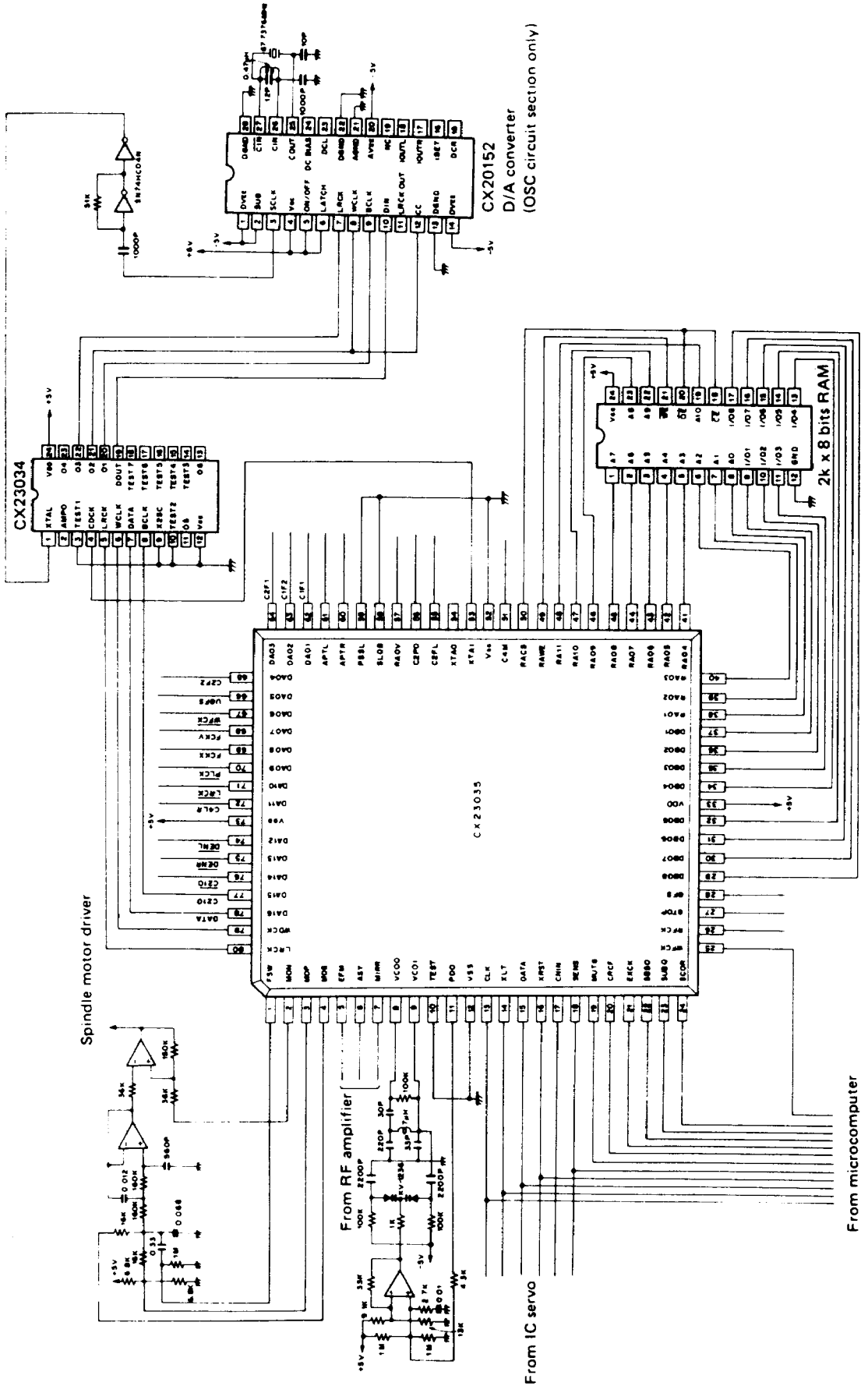


Fig. 4 Band passing characteristics

Example of Application Circuit

(1) Connection of CX23034, CX23035 and CX20152



(2) L-ch and R-ch same phase connection method