YM3623B

Digital Audio Interface Receiver (DIR)

■ OUTLINE

The YM3623B is an LSI device, developed by YAMAHA, which receives and plays back the Digital Audio Interface Format signals that are transferred between digital audio equipment. Use of the YM3623B eliminates the need for a special externally- mounted circuit for playback, thereby greatly facilitating the playback of Digital Audio signals.

■ FUNCTIONS

1) The YM3623B has an internal PLL circuit which synchronizes with the Digital Audio Format signals that are sent in from the external world.
2) It outputs Audio signals starting with the MSB (Most Significant Bit). In sync with that output, it outputs the Timing clocks for the D/A output sample-and-hold operations and the signals indicating the L or R channel.
3) It has a terminal for outputting a Subcode for CD format signal, making possible the retrieval of Subcode data.
4) It is capable of outputting the sampling frequency, Emphasis ON/OFF status, Copy Enable/Disable status, as well as the Error status of transmitted Audio signals.
5) In case an error is detected in the Digital Audio Interface Format signals, the Audio data preceding the detected error is output again.

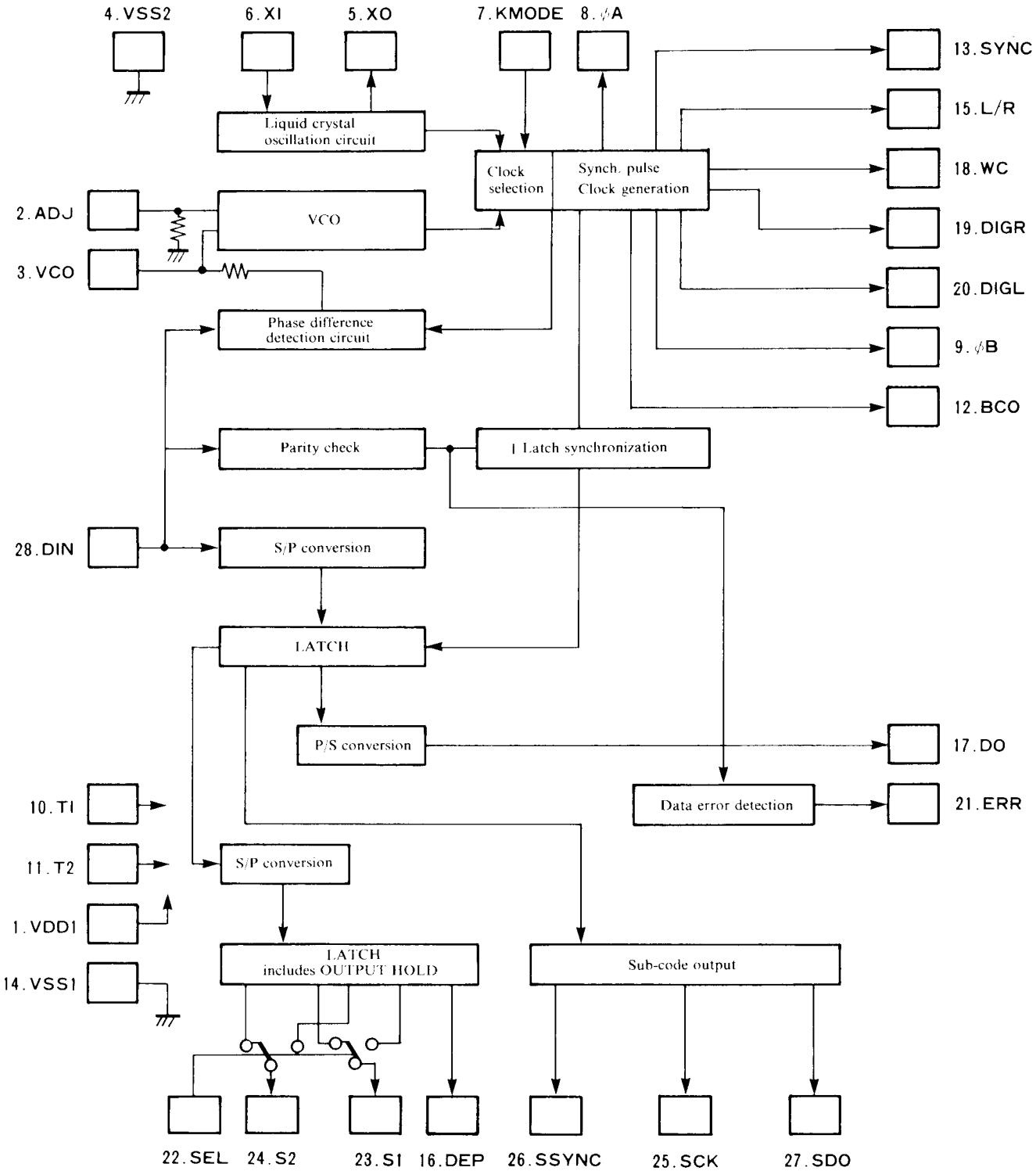
■ FEATURES

1) Silicon gate CMOS construction (low power consumption)
2) 28-pin Dual-Inline Package (DIP)
3) 45V power supply

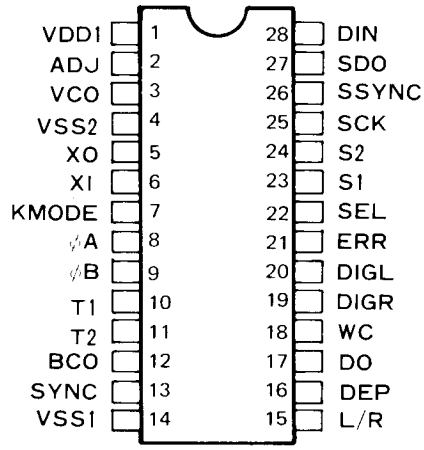
YAMAHA CORPORATION

YM3623B CATALOG
CATALOG No.:LSI-2136233
1991. 10

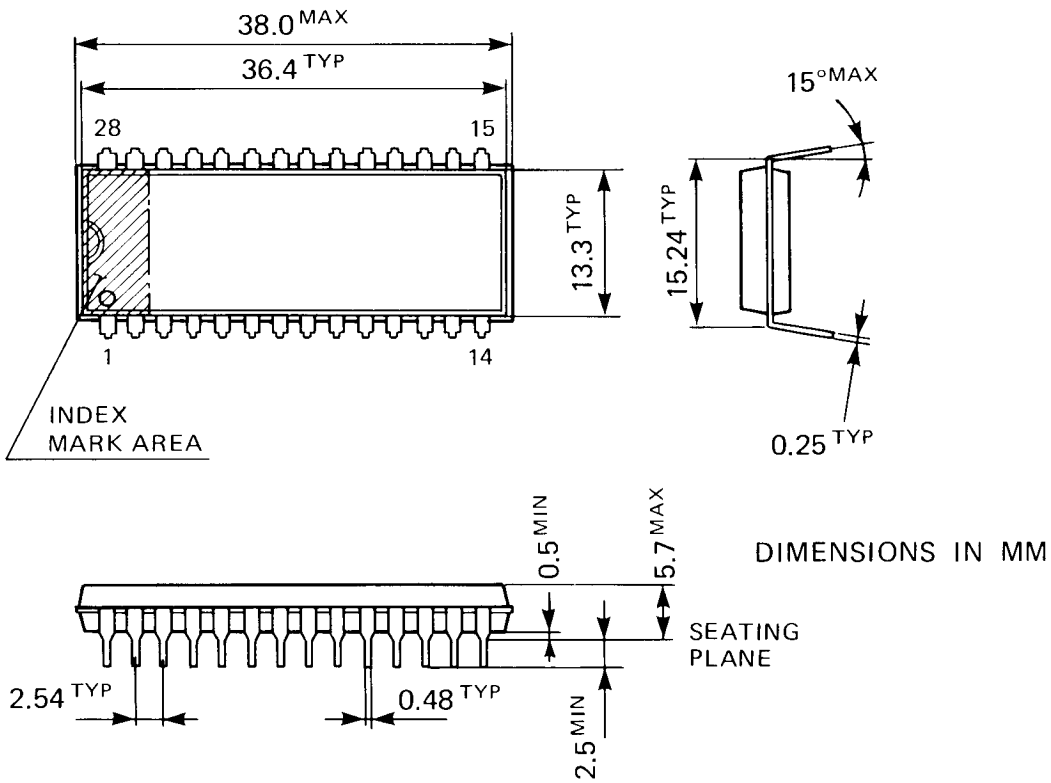
■ BLOCK DIAGRAM



■ PIN ASSIGNMENT DIAGRAM



■ EXTERNAL DIMENSIONS



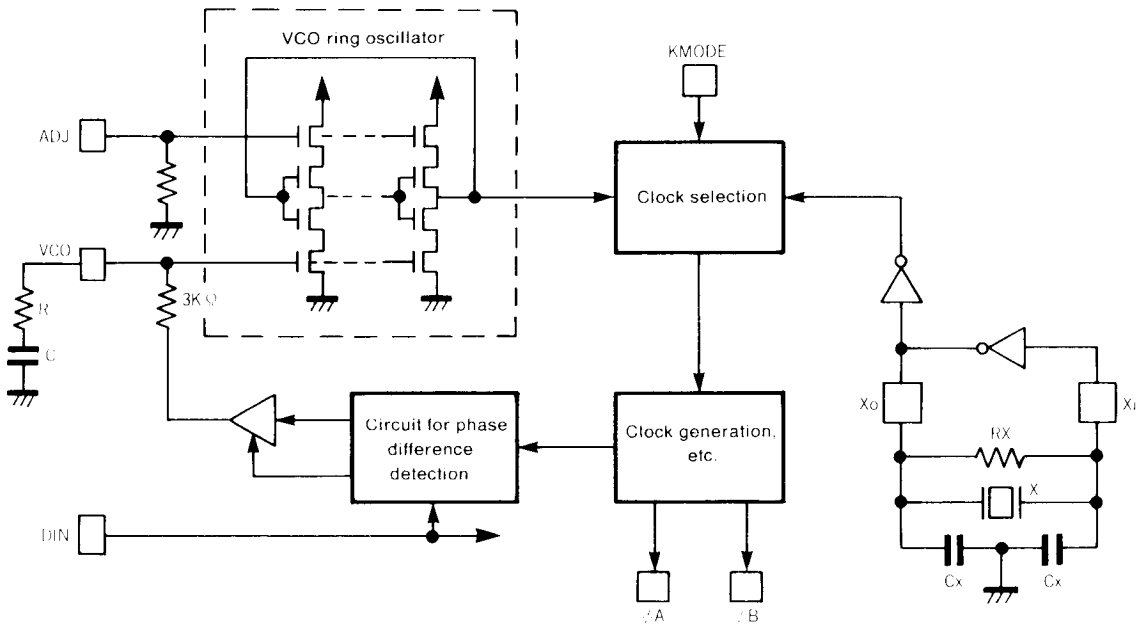
28 pin plastic DIP
PK28DP1-20-1

■ TABLE OF PIN FUNCTIONS

"(PU)" in the I/O column indicates that the terminal is pulled-up internally.

Pin No.	Pin Name	I/O	Function
1	VDD1		System power supply (+5V)
2	ADJ	I	Used for adjusting the VCO oscillating frequency. Not to be connected.
3	VCO	I/O	Externally-connected capacitor pin for the VCO circuit.
4	VSS2		GND for the VCO circuit. To be connected in common with VSS1, since it is not commonly connected within the LSI chip.
5	XO	O	Used for the crystal oscillator element (16.9344MHz - 20MHz).
6	XI	I	Used for the crystal oscillator element, or external clock input terminal
7	$\overline{\text{KMODE}}$	I(PU)	"H": The PLL circuit operates after input from the DIN pin. If no DIN input is received, the crystal oscillator element is selected and operates. "L": The crystal oscillator element is used regardless of the DIN input status.
8	øA	O	Crystal oscillating frequency is output during use of the crystal oscillating element. Changes occur depending on the input speed of DIN pin data while the PLL circuit is operating. (Frequency of input FsX384 when the PLL circuit is locked.)
9	øB	O	1/3 cycle output of øA Changes with the input speed of DIN pin data while the PLL circuit is operating. Frequency of input FsX384 when the PLL circuit is locked.
10	$\overline{\text{T1}}$	I(PU)	Used for checking the internal circuitry. Not to be connected.
11	$\overline{\text{T2}}$	I(PU)	Used for checking the internal circuitry. Not to be connected.
12	BCO	O	Timing clock for the signals output from the DO pin.
13	$\overline{\text{SYNC}}$	O	Sync signal for DO output.
14	VSS1	O	System GND (+0V).
15	L/R	O	L/R Latch signal for DO output. Indicates that L Channel data ("H") or R Channel data ("L") will be output from the DO pin.
16	DEP	O	De-emphasis output re-generated from user bits. "H": Indicates that input data was subjected to emphasizing. "L": Indicates that input data was not subjected to emphasizing.
17	DO	O	16-bit audio data output.
18	WC	O	Word clock output from the DO pin.
19	DIGR	O	R Channel Deglitch signal.
20	DIGL	O	L Channel Deglitch signal.
21	ERR	O	"H": Indicates a parity error or crystal operation. "L": No error.
22	SEL	I(PU)	See the following table.
23	S1	O	See the following table.
24	S2	O	See the following table.
25	SCK	O	Bit clock for Subcode output.
26	SSYNC	O	Sync signal for Subcodes.
27	SDO	O	Terminal for Subcode data output.
28	DIN	I(PU)	Terminal for data input. (EIAJ format signal is input.)

■ CLOCK



R 100Ω ~ 300Ω
C 2,000PF ~ 10,000PF

RX : 1MΩ
CX 5 ~ 20PF
X : 16MHz ~ 20MHz

Block diagram of clock circuit

• Switching clock

This chip has a VCO mode and a Crystal mode, which switch each system clock.

- VCO mode is enabled when data is input at DIN, and the received signal is transmitted from an output pin during the PLL process.
- Crystal mode is a "wait" status where the operation is internally performed with a crystal clock and signals transmitted from output terminals have no significance.

* The $\overline{\text{KMODE}}$ pin switches between these two modes.

- VCO mode is entered only when the $\overline{\text{KMODE}}$ pin is "H" and correctly-formatted data is input to the DIN pin.
  In this mode, the internal VCO operates by re-generating the clock from the data input to the DIN pin. At this time, a parity check is internally performed, and the ERR pin goes "L" if no error has been detected.
- Setting the $\overline{\text{KMODE}}$ pin to "L" switches the mode to crystal operation, regardless of any input at the DIN terminal. In this case, the ERR pin always stays "H".
- The $\overline{\text{KMODE}}$ pin is also used for internal reset when the power is turned on. Therefore, this pin should be set to "L" at least once when the power is turned on, before the PLL circuit is locked.
  The minimum time required to hold the $\overline{\text{KMODE}}$ pin "L" equals the time for the internal LSI circuitry to charge the external time constant circuit, using the voltage which is output from the VCO pin.
- If the DIN input signal is interrupted, and no further changes occur, then VCO mode changes to Crystal mode automatically.

• VCO OPERATION

A PLL circuit is built in, so that the sync clock is re-generated from the signal input to the DIN pin. The VCO works as a high- frequency ring oscillator when operating in free-running mode.

During operation of the PLL, a pulse string is transmitted from the VCO pin as a result of phase comparison in the phase difference detection circuit. This string is integrated in the externally attached CR and defined as the control voltage of the VCO oscillation circuit. As shown in the block diagram of the clock circuit, this becomes a gate voltage for the inverter of the ring oscillator circuit. The gate voltage changes with respect to resistance changes → delay time changes → oscillation frequency changes in this order. The oscillation frequency changes are reflected into the phase comparator as feedback.

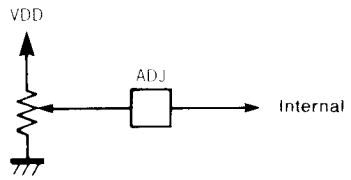
The VCO frequency appears at the øA terminal in the VCO mode, and in the crystal mode, the oscillation frequency at the øA terminal equals that of the input clock at the XI terminal.

The VCO oscillation frequency is related to the delay time of the element in the VCO oscillation circuit. Therefore, the frequency tends to fluctuate depending on changes in temperature or power source voltage. The time constant for the VCO pin needs to be reviewed, taking individual component differences into account.

With regard to the CR time constant circuit which is needed for leading-in the PLL, the PLL circuit tends to become unlocked when R is high (approx. 300 ohms or more) and there is a high input rate at the DIN pin. On the other hand, the PLL circuit tends to be locked in the wrong way when R is low and C is high (approx. R = 100 ohms or less, and C = 0.015 μF or more).

The VCO time constant which causes lead-in to the input sampling rate 48KHz-32KHz should fall within the range of 100-270 ohms + 2000-8000pF.

- The ADJ pin should not be connected.
  In order to adjust the VCO free-running frequency, apply a DC bias with a range between 0V and VDD to the ADJ pin.
  To check the VCO in free-running mode, output the VCO free- running frequency from the øA pin by setting $\overline{T1}$ to "L", $\overline{T2}$ to "L", DIN to "L" and $\overline{KMODE}$ to "H".



Example of VCO free-run adjustment circuit

■ S1, S2, SEL, DEP

S1, S2 and DEP pins retransmit the channel status from the DIN input signal (EIAJ format). The SEL pin switches the functions of the S1 and S2 pins.

• S1 and S2 output when SEL = "L"

S1	Function
L	Copy disabled
H	Copy enabled

S2	Function
L	Other than DAT
H	DAT

The S1 pin outputs bit 2 of the channel status: control code(COPY). S2 pin output represents bit 8 and bit 9 (category code) of the channel status. When bit 8 and bit 9 are both equal to 1, S2 goes "H". Otherwise, S2 goes "L".

• S1 and S2 output when SEL = "H"

S1	S2	Function (Sampling frequency)
L	L	Sampling frequency: 44.1KHz
L	H	Sampling frequency: 48KHz
H	H	Sampling frequency: 32KHz
H	L	——— (reserved)

Both pins reflect bit 24 and bit 25 (sampling frequency) of channel status. (S1 = bit24, S2 = bit25)

• DEP pin output

When the control code (bit 0-5) of channel status is "X0X100", DEP goes "H". Otherwise, DEP = "L" is output.

■ ERR pin output

ERR = "H" during operation in the crystal mode or with parity error. ERR = "L" in the VCO mode with no parity errors.
The V flag does not affect the ERR pin.
Attention should be paid when using ERR pin output, since this output fluctuates while switching from the crystal mode to the VCO mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Units
Supply voltage	V_{DD}—V_{SS}	−0.3 ~ +7.0	V
Input voltage	V_I	V_{SS} − 0.3 ~ V_{DD} + 0.5	V
Operating temperature	T_{OP}	−20 ~ +75	°C
Storage temperature	Tstg	−50 ~ +125	°C

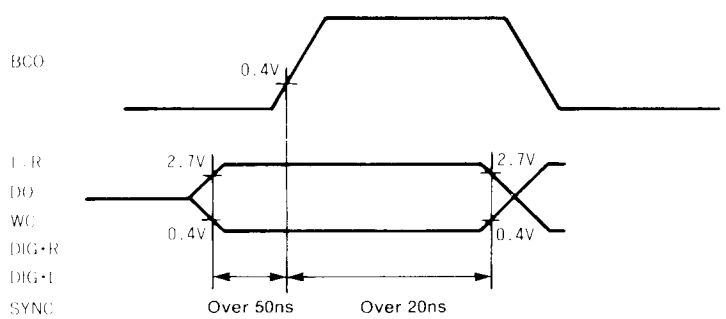
2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}—V_{SS}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

3. Electrical Characteristics

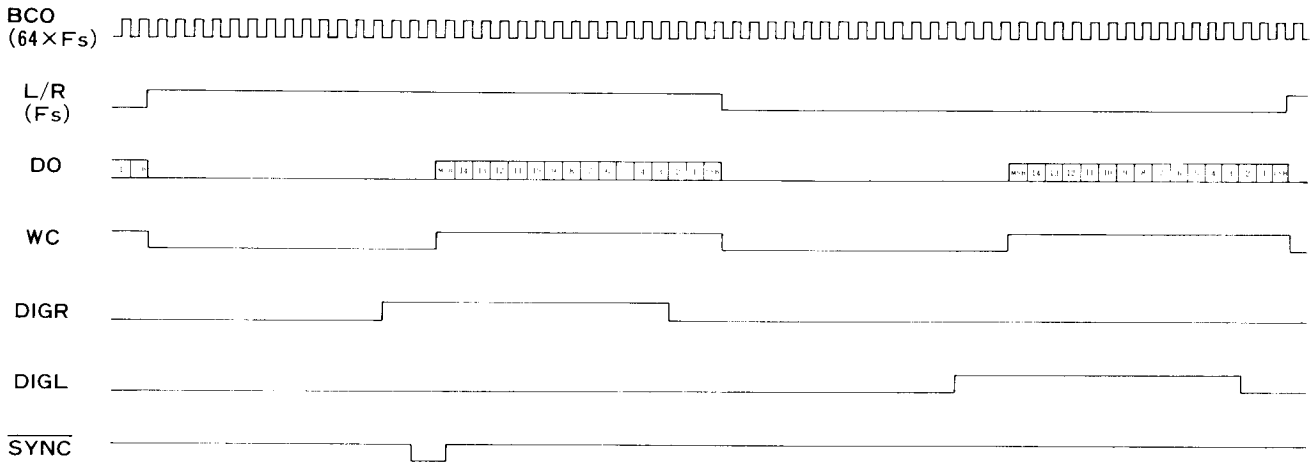
Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	V_{DD} = 5V D_{IN} = 5V fc = 16.9344MHz		6	8	mA
High-level output voltage	V_{OH}	I_{OH} = 0.4mA	4.0			V
Low-level output voltage	V_{OL}	I_{OL} = 2mA			0.4	V
High-level input voltage	V_{IH}	X_I pin excluded X_I pin	2.0 4.5			V
Low-level input voltage	V_{IL}				0.8	V
Input leakage current	I_{LK}	V_I = 5V			10	μA

NOTE: Analog VCO and ADJ terminals are excluded.



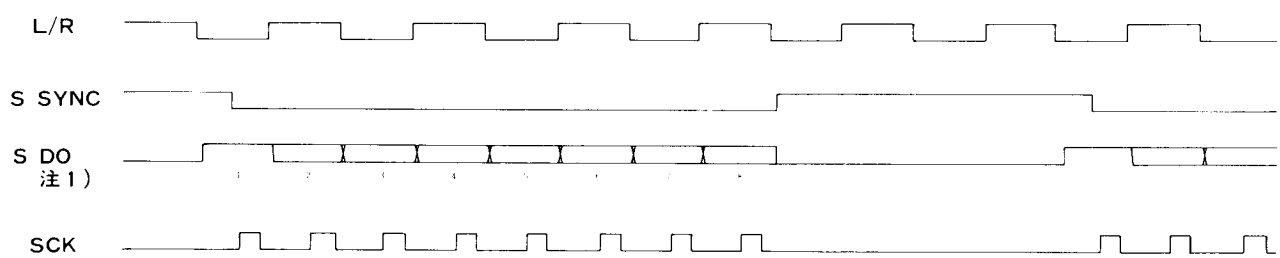
Output timing

OUTPUT TIMING (1)



NOTE: "Fs" represents the sampling frequency. For a compact disk, for example, Fs = 441.1KHz.

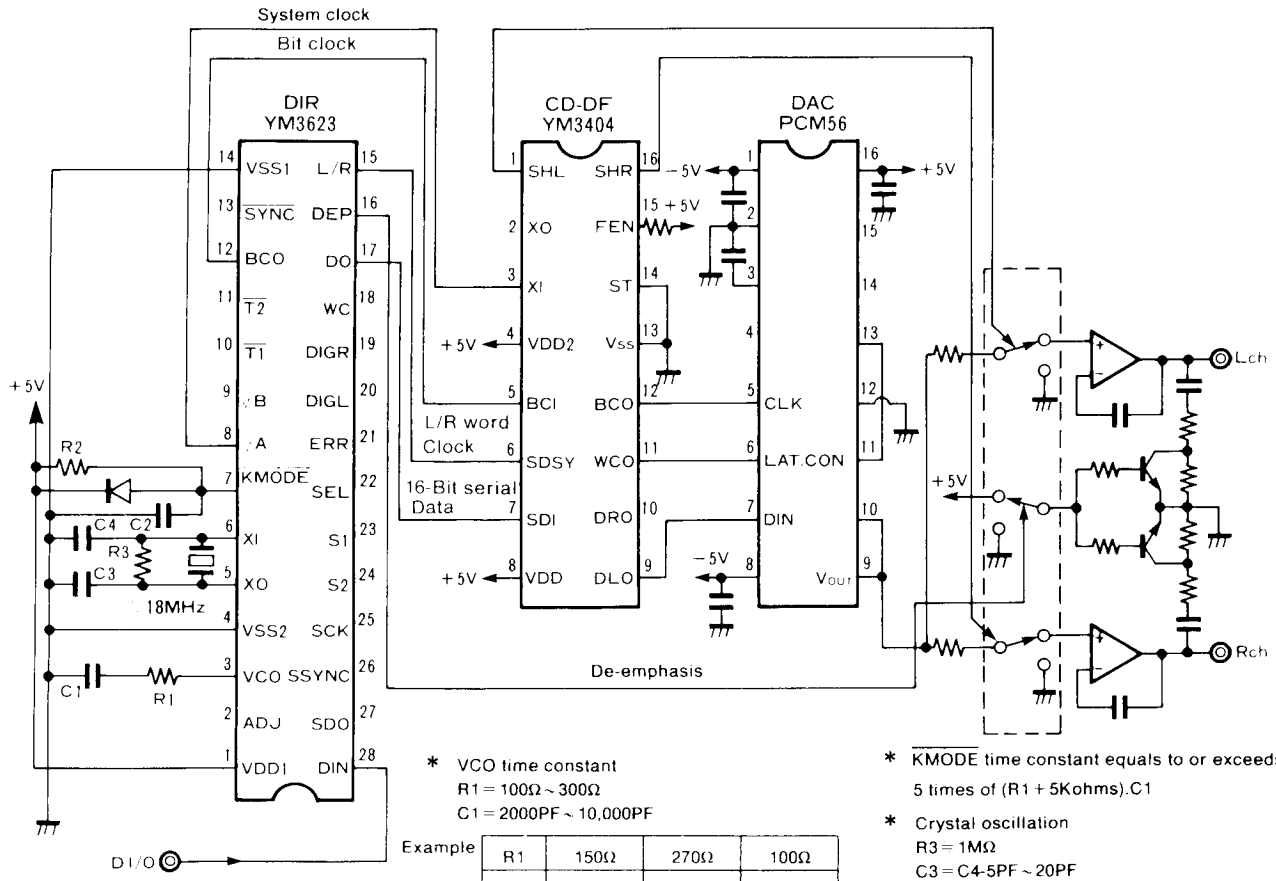
OUTPUT TIMING (2)



NOTE 1: When the "U" bit that is input by DIN becomes "1", eight "U" bits will be directly output to SDO.

NOTE 2: The above timing chart is a typical example. SDO will start from the L or R channel according to the data timing of the "U" bit input by DIN, then will change during the interval following the eight-bit output until the output of the next eight bits.

■ APPLICATION



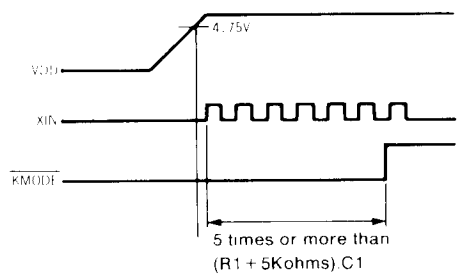
* VCO time constant
R1 = 100Ω ~ 300Ω
C1 = 2000PF ~ 10,000PF

Example	R1	150Ω	270Ω	100Ω
	C1	4700PF	8200PF	8200PF

* $\overline{\text{KMODE}}$ time constant equals to or exceeds 5 times of (R1 + 5Kohms).C1

* Crystal oscillation
R3 = 1MΩ
C3 = C4-5PF ~ 20PF

The holding of $\overline{\text{KMODE}}$ at "L" required for reset at power-on should be performed for a period of time 5 times or more than (R1 + 5Kohms).C1 time constant, after VDD exceeds 4.75V and the Xi clock is input.



The specifications of this product are subject to improvement changes without prior notice.

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