YM3414

(ACDDF)

2-Channel 8-times Oversampling Digital Filter

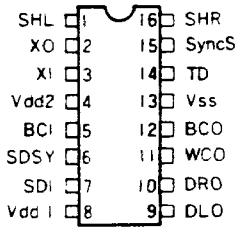
■ OUTLINE

The YM3414 (ACDDF) is a super-high performance 8-times oversampling digital filter for use with the digital audio systems developed by Yamaha.
It is connectable directly to LSI, DIT, DIR, etc. for digital audio systems, and can exhibit its exellent performance through simple procedures.

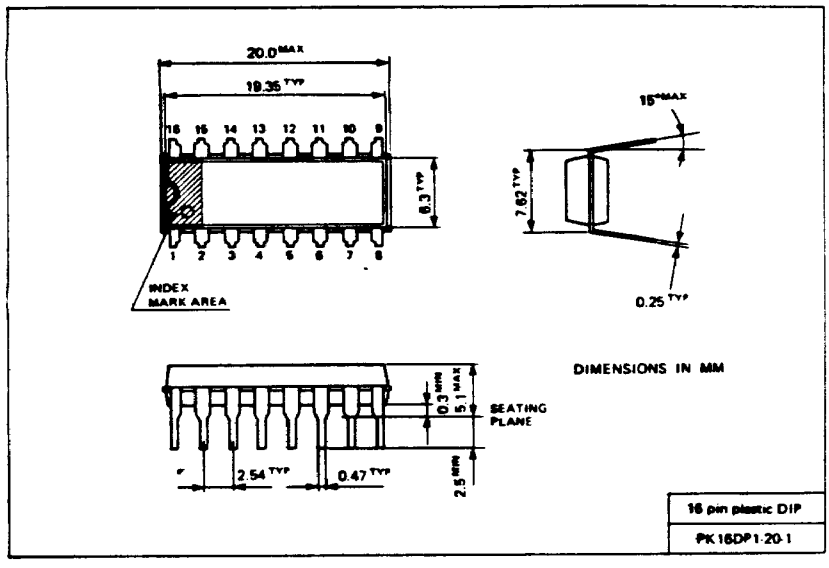
■ FEATURES

- 8-times oversampling in two channels
- Linear phase FIR type filters connected in three vertical stages
  - 1'st filter: 225-order FIR filter
  - 2'nd filter: 41-order FIR filter
  - 3'rd filter: 21-order FIR filter
- 19 × 18 bits multiplier built in
- Floating point multiplier and accumlater having a coefficient of 18 bits
- Overflow limiter built in
- Filter characteristics (fs=44.1 kHz)
  - Pass band ripple: Within ±0.0001 dB at 0 to 20 kHz
    (Within quatization error in 16 bits)
  - Stop band attenuation: At least 100 dB at 24.1 kHz and higher
- High precision oscillator specially designed for use with the filter
- C-MOS type processor
- Single 5 V power supply
- 16-pin type DIP package

■ TERMINAL DIAGRAM



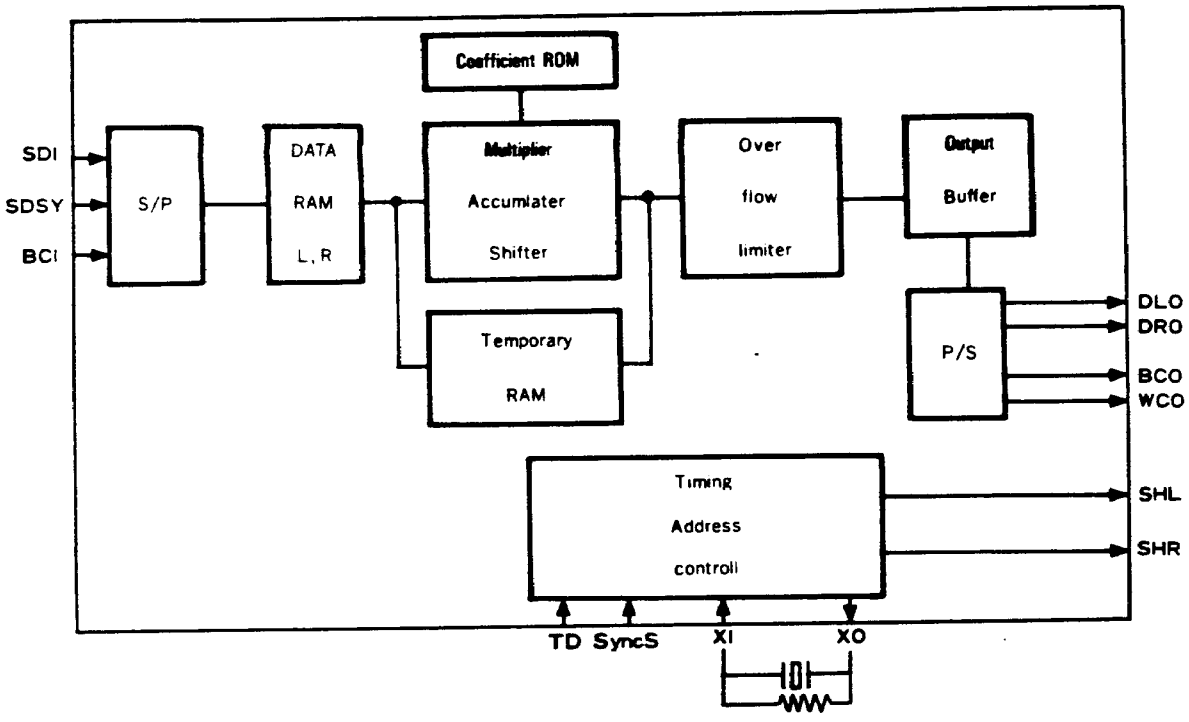
■ TERMINAL FUNCTIONS



■ EXTERNAL DIMENSIONS

Terminal Name	Pin No.	I/O	Outline of Functions
SHL	1	O	At 1 DAC (TD='L'): Degricher signal for Lch (At 4-times) At 2 DAC (TD='H'): Degricher signal for L/Rch (At 8-times)
XO	2	O	Crystal oscillation between XI-XO.
XI	3	I	Clock rate is 384 fs (and can be fed direct to X1)
Vdd2	4		+5 V power supply terminal for crystal oscillation and degricher signal
BCI	5	I	Bit clock input terminal for input data
SDSY	6	I	Clock signal indicating L/Rch discrimination of input data and input timing
SDI	7	I	Data input terminal
Vddl	8		+5 V power supply terminal for the digital signal system
DLO	9	O	At 1 DAC (TD='L'): L and Rch data output terminal (At 4-times) At 2 DAC (TD='H'): Lch data output terminal (At 8-times)
DRO	10	O	Rch data output terminal
WCO	11	O	Word clock for output data DLO and DRO
BCO	12	O	Bit clock for the output data.
Vss	13		GND terminal
TD	14	I	1 DAC/2 DAC switching terminal (1 DAC (At 4-times)='L', 2 DAC (At 8-times)='H')
SyncS	15	I	Sync signal for absorbing jitter in asynchronous input (SyncS="H" for complete sync input; SyncS="L" for inhibiting SDSY)
SHR	16	O	Rch degricher signal at 1 DAC

■ BLOCK DIAGRAM



■ OUTLINE OF FUNCTIONS

The functions of the 2-channel 8-times oversampling digital filter are obtained by connecting linear phase type of FIR filters at three vertical stages: 225-order FIR filter at the first stage and 41-order FIR filter at the second stage and 21-order FIR filter at the last stage.
The built-in multiplier is of 19 × 18 bits type and comprises an overflow limiter. It performs multiplication and addition with floating point in 18 bits of coefficient wordlength.
Theoretical filter characteristics are: (fs=44.1 kHz)

Ripple at pass band (0 to 20 kHz): Within 0.0001 dB or below quantization error in 16 bits

Attenuation at stop band (24.1 kHz): At least 100 dB

The sampling digital filter can process input of MSB first 2's in 16 bits 2 channels.
Output is obtainable in the signal format of 1 DAC or 2 DAC depending on setting of TD. TD held "L" (for 1 DAC) is for 4-time oversampling; TD held "H" (for 2 DAC) is for 8-times oversampling. Extended portion of the internal multiplication data is output to the two bits (−2) and (−1) below LSB. The data is unnecessary for operation of the sampling digital filter in 16 bits. The filter is so designed as to minimize rounding error at any omitting position.

	fs = at 44.1KHz	fs standard
Ripple at pass band	within 0.0001dB	
Pass band	0~20KHz	$0 \sim \frac{20}{44.1} \cdot fs$
Attenuation at stop band	within −100dB	
Stop band (at 4-times)	24.1−328.7KHz	$\frac{24.1}{44.1} \cdot fs \sim \frac{328.7}{44.1} \cdot fs$
" (at 8-times)	24.1−152.3KHz	$\frac{24.1}{44.1} \cdot fs \sim \frac{152.3}{44.1} \cdot fs$

	fs = at 44.1KHz	fs standard
Slope characteristics	at 8-times: 0.00016dB at 4-times: −0.00013dB	
	20KHz	$\frac{20}{44.1} \cdot fs$
	at 8-times: 0.00016dB at 4-times: −0.00013dB	
	24.1KHz	$\frac{24.1}{44.1} \cdot fs$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	VDD	−0.3	+7.0	V
Input voltage	VI	−0.3	Vdd+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

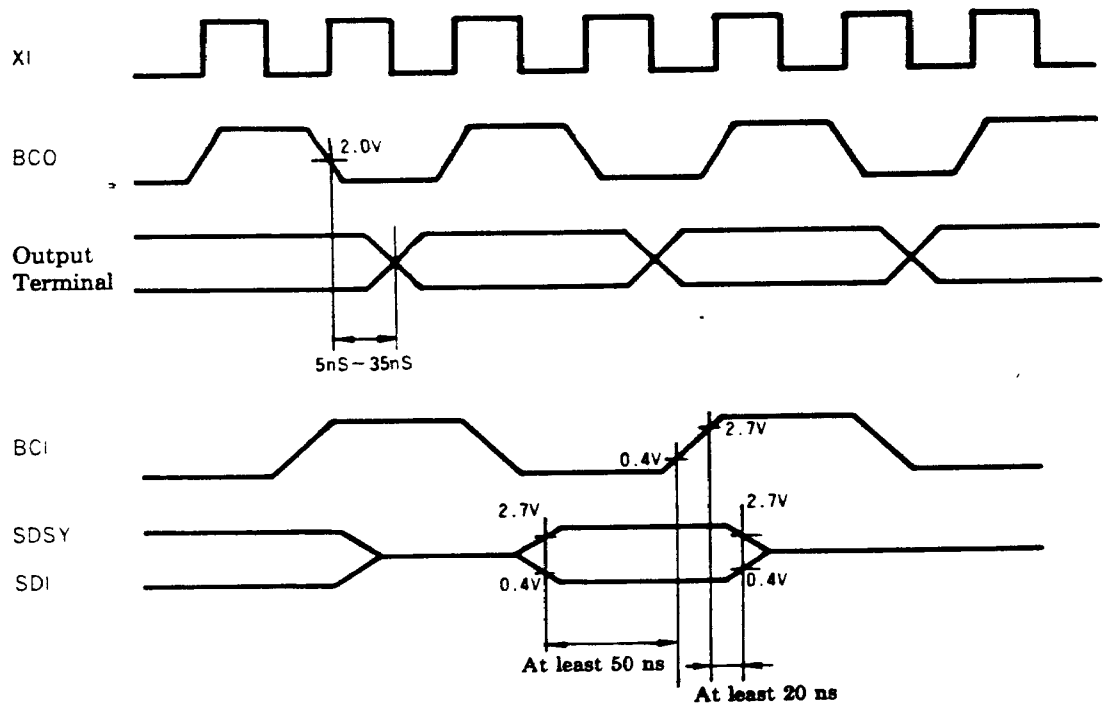
■ RECOMMENDED WORKING CONDITIONS

Item	Symbol	Minimum	Standard	Maximum	Unit
Power supply voltage	VDD	4.75	5.0	5.25	V
Clock frequency	XIN	12.2	16.93	18.5	MHz
Working temperature	Top	0	25	70	°C

■ ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 ± 0.25 V)

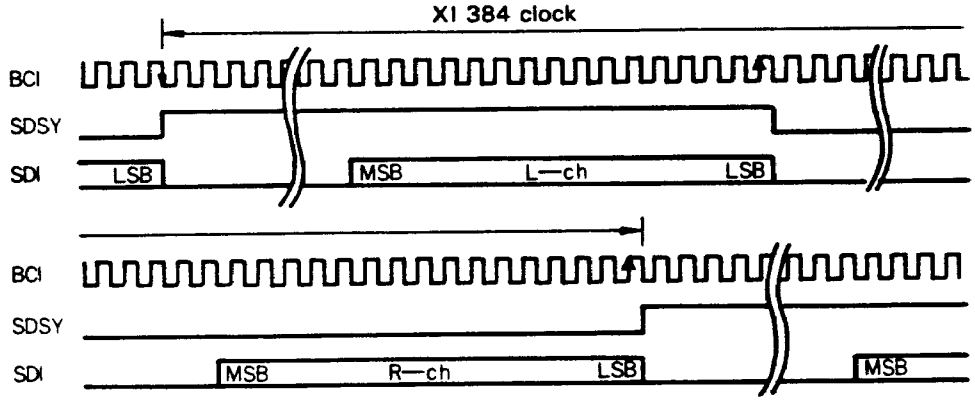
Item	Symbol	Condition	Minimum	Standard	Maximum	Unit
Power consumption	W	Vdd=+5V		200	270	mW
Input voltage H level (XI, TD) (BCI, SDSY, SDI, SyncS)	VIH		 3.5 2.7		 Vdd Vdd	 V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		Vdd	V
Output voltage L level	VOL		0		0.4	V
Output delay (delay from BCO)			5		35	nsec
Input data setup time (Rise of BCI)			50			nsec
Input data hold time (Rise of BCI)			20			nsec
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ TIMING CHART

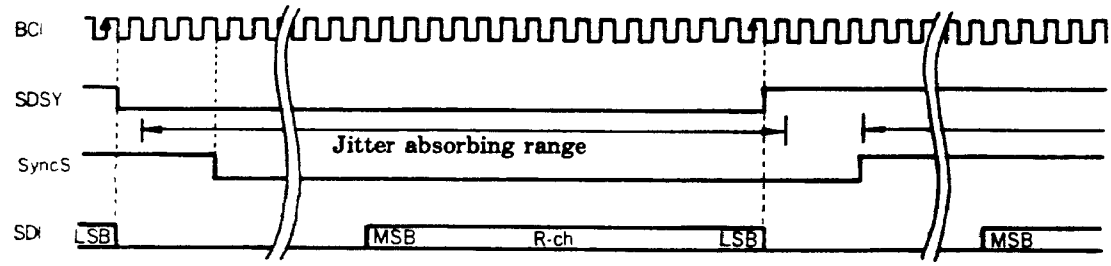


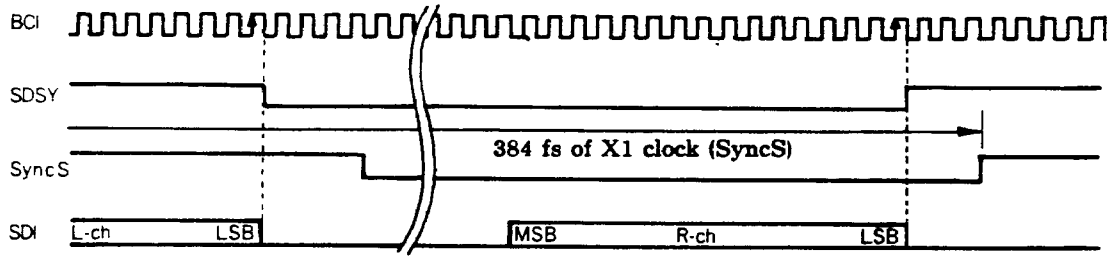
■ INPUT SIGNAL FORMAT

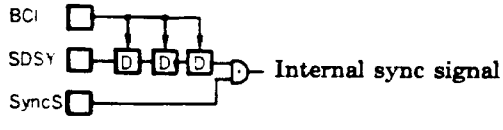
■ 98fs (FEN = "L")



SyncS = "H"
During the rise-to-rise interval of SDSY, any clock may be applied to BCI terminal provided that X1 clock be 384 fs. Signals BCI, SDSY and SDI are to be in complete synchronism with X1 clock and, for this reason, their frequencies must be obtained by frequency-division of X1 frequency, there being no requirement on the phase relationship of these with X1. Both SDSY and SDI go into synchronism by rising.



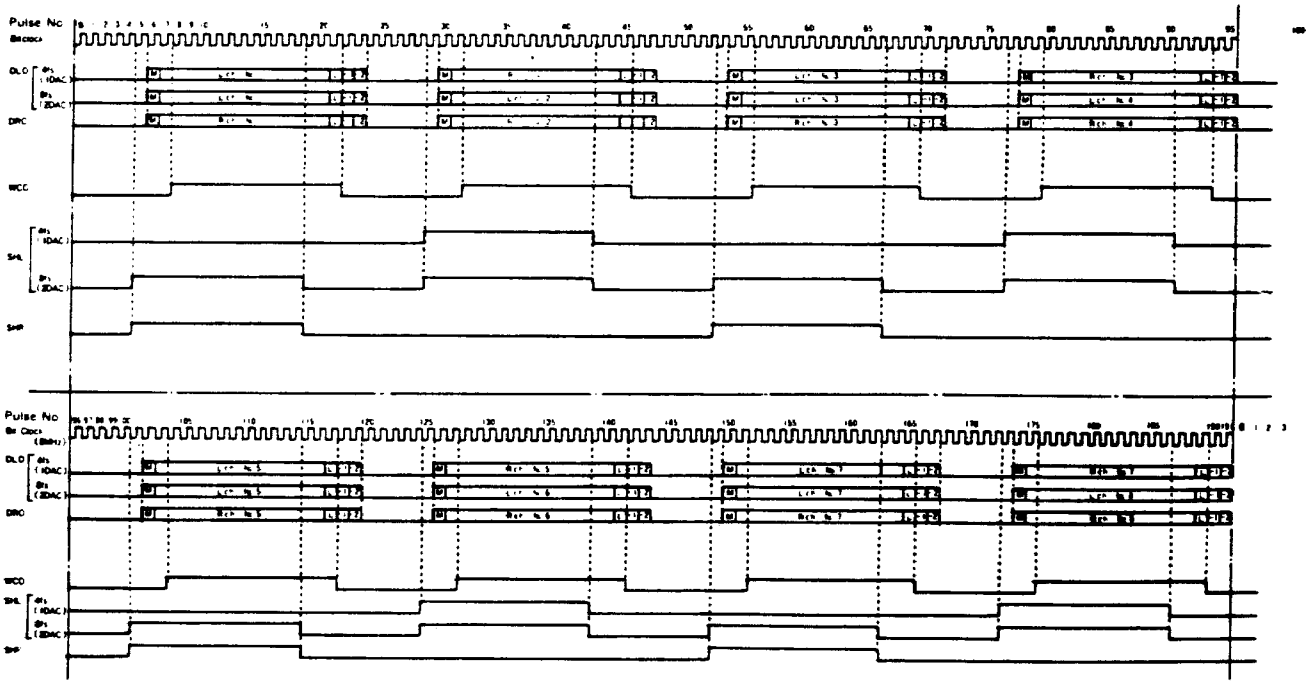




Asynchronous inputs

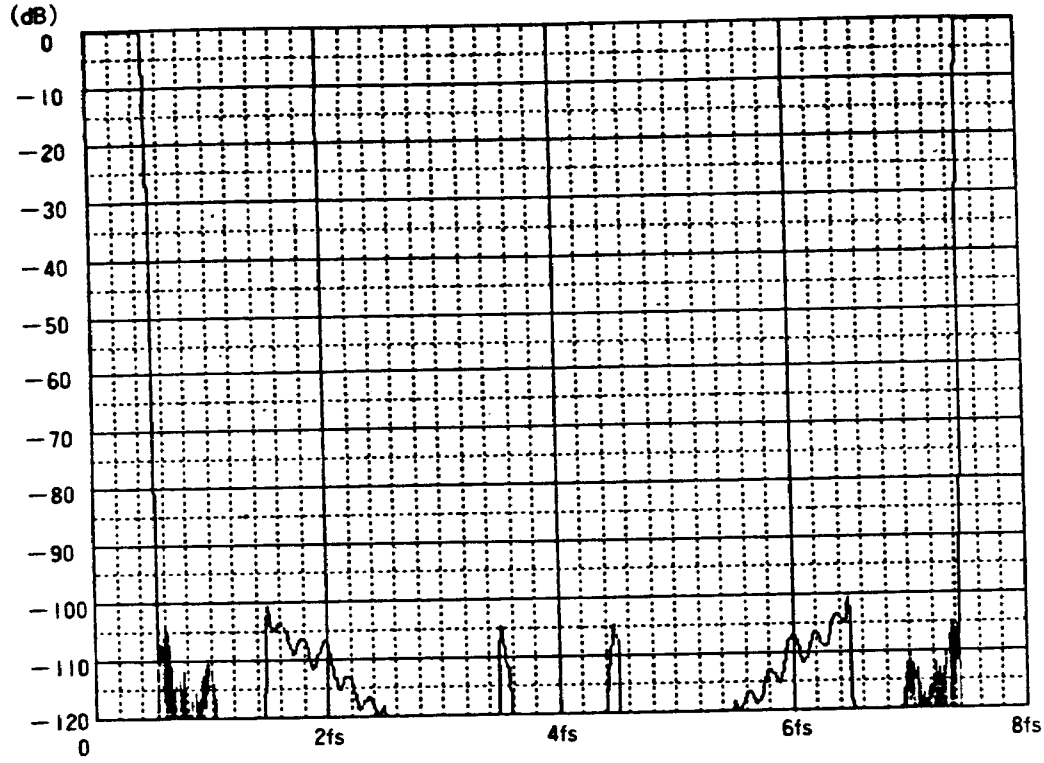
SyncS signal is to mask SDSY signal. In other words, SDSY is to be delayed by 3 pulses of BCI and by anding the delayed SDSY and syncS signal to produce a start signal for internal computation. This explains why syncS signal and X1 clock have to be in complete synchronism and why some jitter is allowed in signals SDSY, BCI and SDI.

■ OUTPUT SIGNAL FORMAT

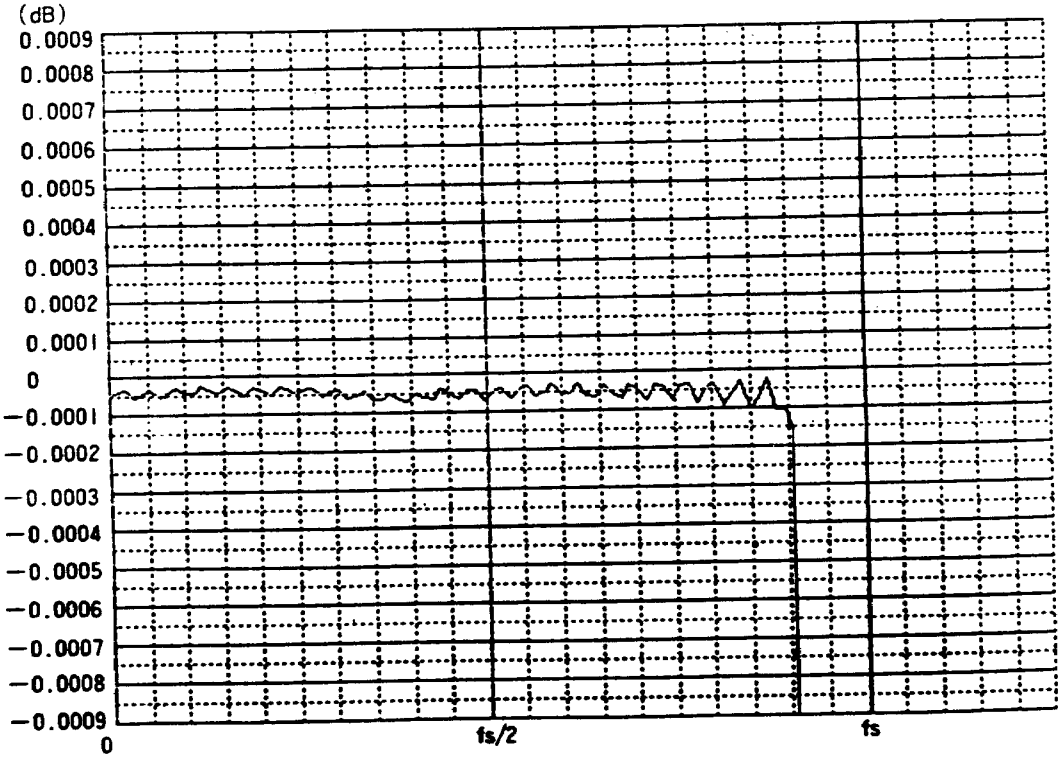


■ CHARACTERISTICS FOR REFERENCE

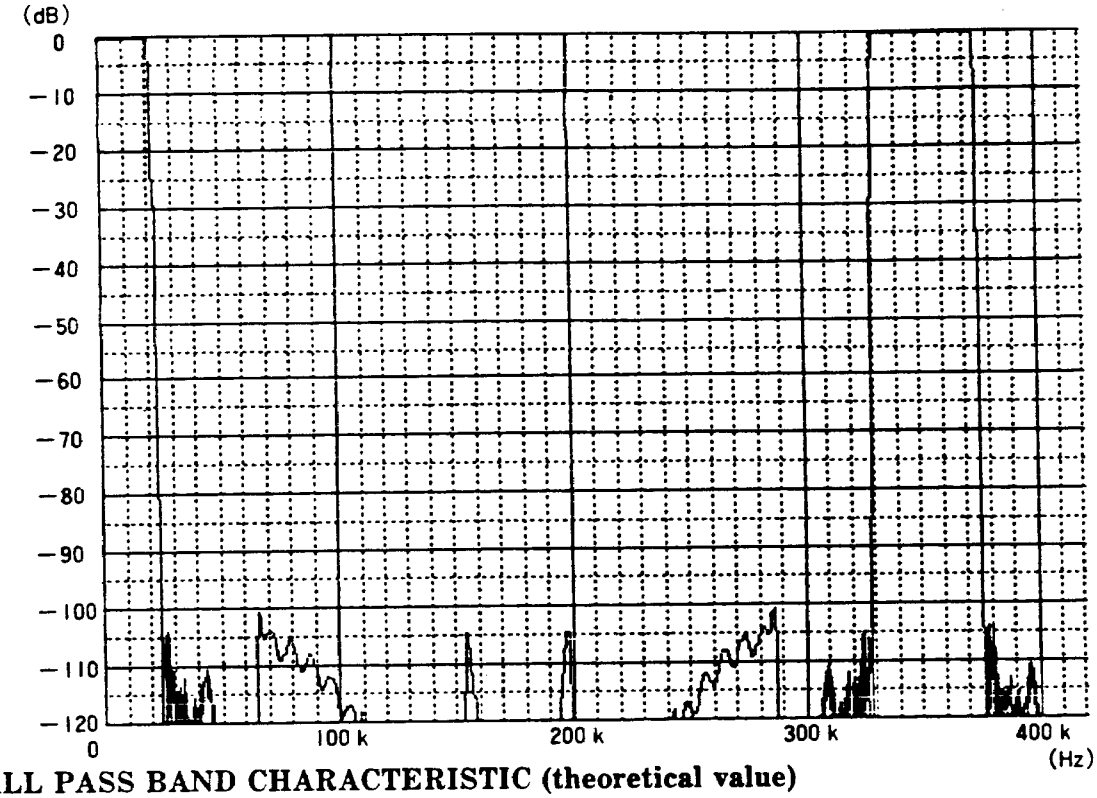
OVERALL CHARACTERISTIC (theoretical value)



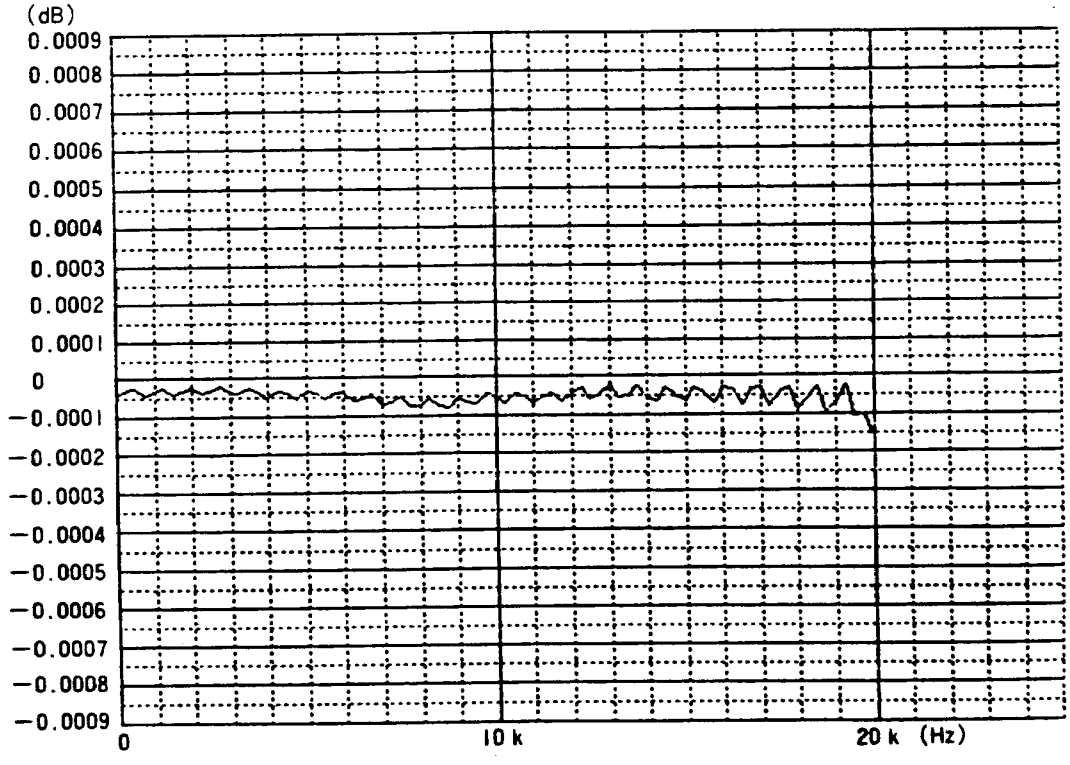
OVERALL PASS BAND CHARACTERISTIC (theoretical value)



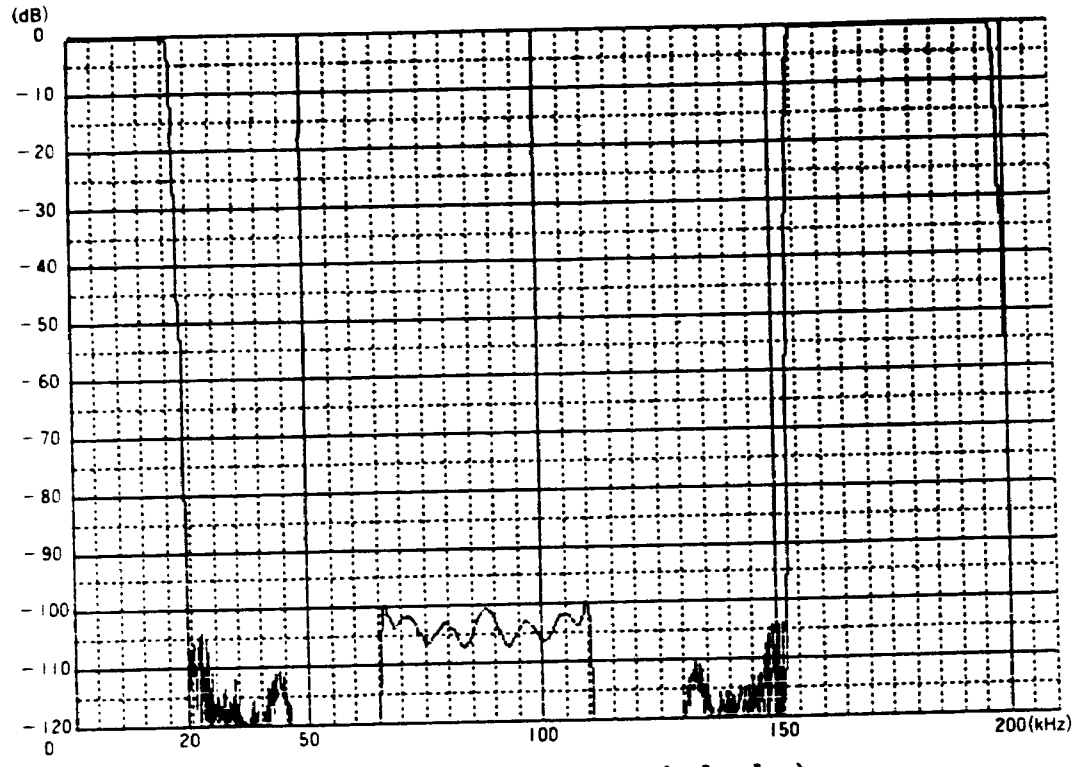
OVERALL CHARACTERISTIC theoretical value (fs = 44.1 kHz At 8-times)



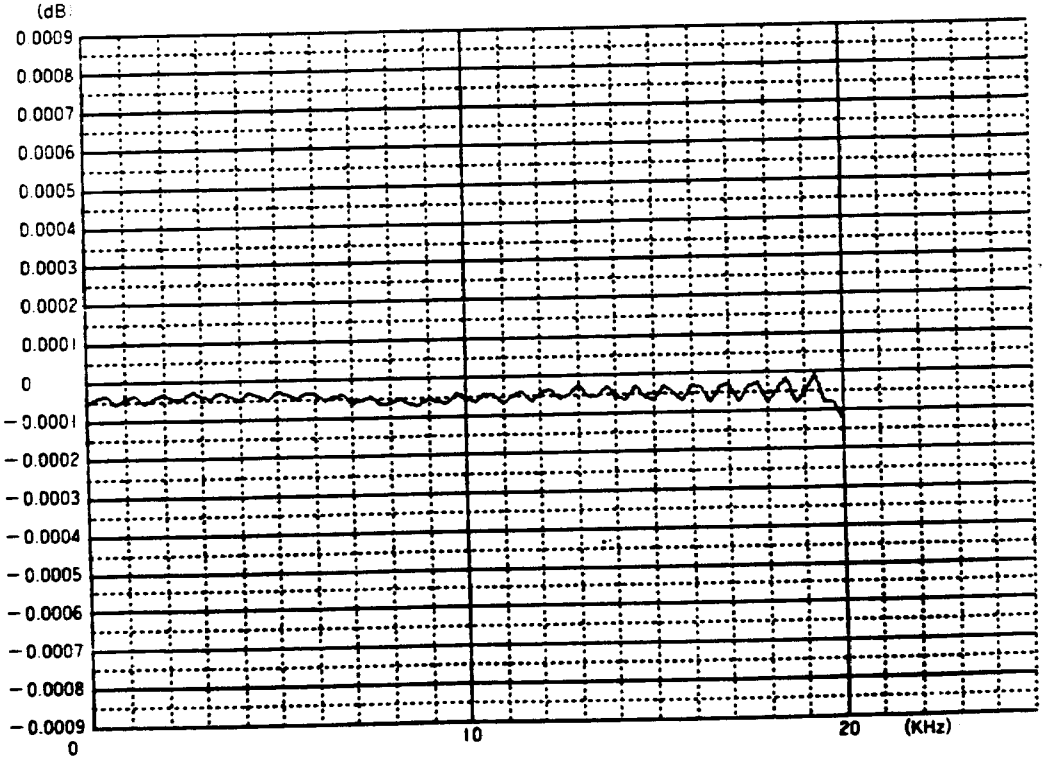
OVERALL PASS BAND CHARACTERISTIC (theoretical value)



OVERALL CHARACTERISTIC theoretical value (fs = 44.1 kHz At 4-times)

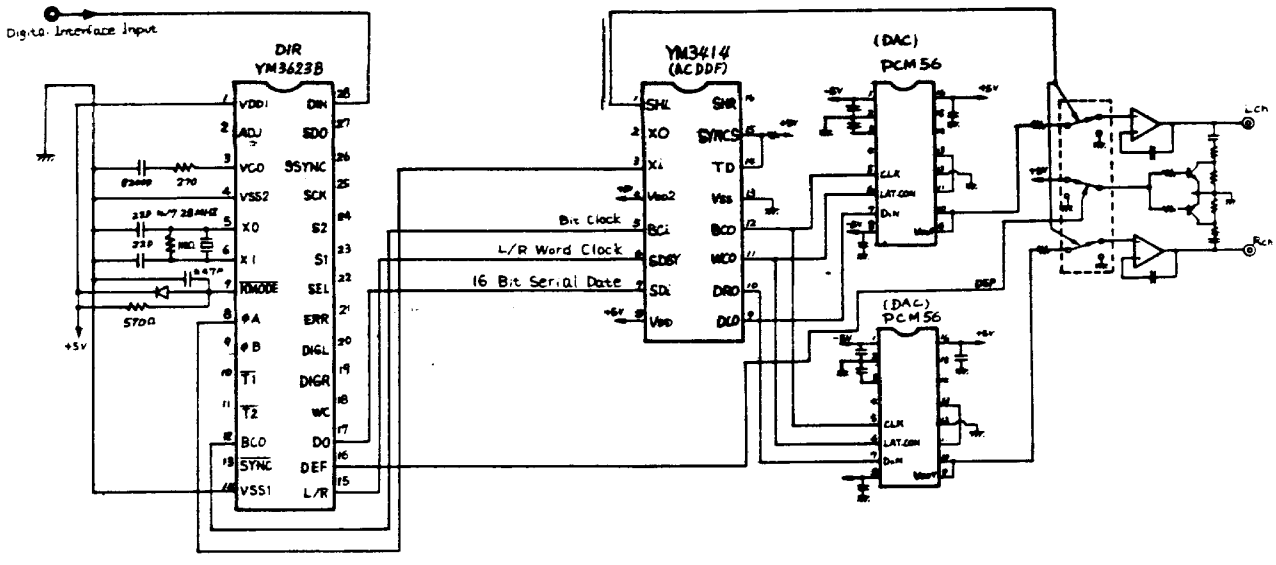


OVERALL PASS BAND CHARACTERISTIC (theoretical value)

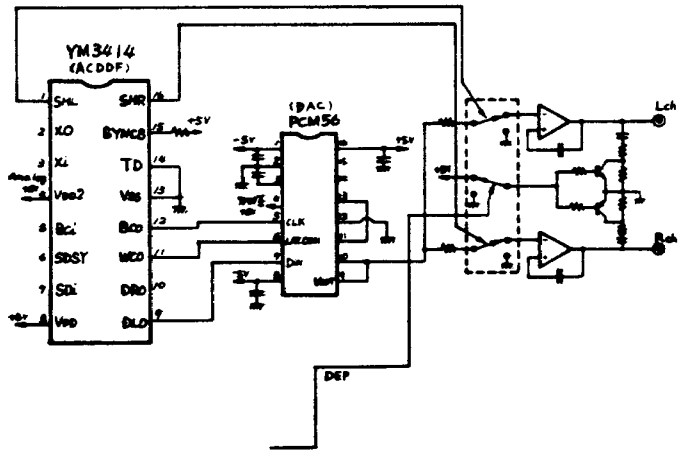


■ EXAMPLES OF APPLICATION

System (8-times Oversampling)



1 DAC System (4-times Oversampling)



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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