FILTER CIRCUIT FOR COMPACT DISC — SAA7030

GENERAL DESCRIPTION

The SAA7030 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. The circuit incorporates two identical filters, each with a sampling rate of four times that of the normal digital audio sampling.

Features

- Suppresses spurious lobes in the audio spectrum
- Improves the signal quality for digital-to-analogue conversion
- Allows a low-order analogue post filter to be used after the digital-to-analogue convertor (DAC)
- Option of offset binary or two's complement data output format
- Electrically-selectable d.c. offset/no offset on data output
- Overflow detection and protection
- Directly compatible with the interpolation and muting circuit (SAA7000)
- Generates a latch output strobe to the DAC

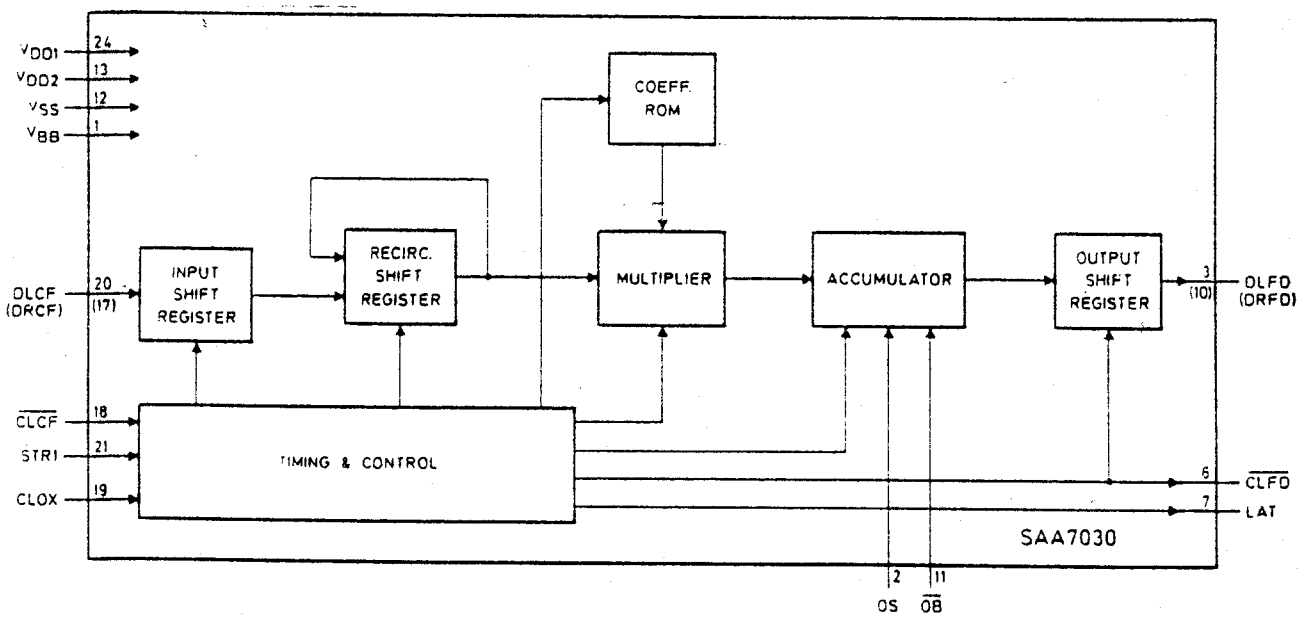


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

FILTER CIRCUIT FOR COMPACT DISC

SAA7030

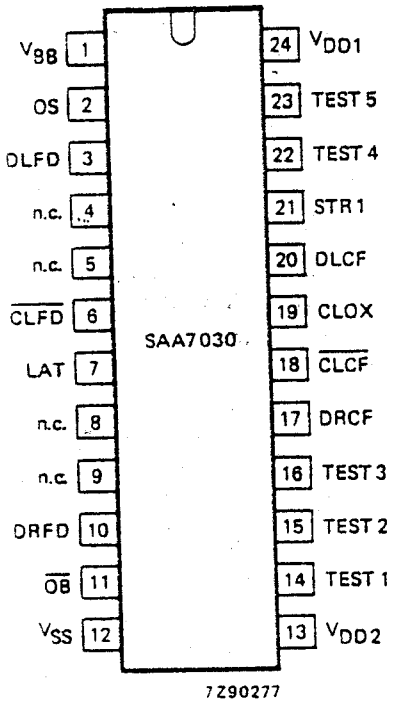


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	OS	offset/no offset select input
3	DLFD	left channel data output
4	n.c.	not connected
5	n.c.	not connected
6	$\overline{CLFD}$	data clock output
7	LAT	strobe output
8	n.c.	not connected
9	n.c.	not connected
10	DRFD	right channel data output
11	$\overline{OB}$	offset binary/two's complement select input
12	V_{SS}	ground
13	V_{DD2}	+ 12 V supply
14	TEST1	test output
15	TEST2	test input
16	TEST3	test input
17	DRCF	right channel data input
18	$\overline{CLCF}$	data clock input
19	CLOX	master clock input
20	DLCF	left channel data input
21	STR1	strobe input
22	TEST4	test input
23	TEST5	test input
24	V_{DD1}	+ 5 V supply

3

FUNCTIONAL DESCRIPTION

The SAA7030 is a stereo interpolating filter which quadruples the data sample rate from 44,1 to 176,4 kHz and thus achieves the following:

1. It suppresses spurious spectrum lobes in the output data that occur between the baseband frequency and 176,4 ± 20 kHz. This allows the DAC to be followed by a low-cost filter of the linear phase, low order, analogue post filter type (a very high order, low-pass filter would otherwise be required to suppress the 44,1 ± 20 kHz lobe).
2. It performs noise-shaping so that a 14-bit DAC yields the same in-band quantizing signal-to-noise ratio as from a 16-bit DAC supplied with unprocessed 44,1 kHz samples.

FILTER CIRCUIT FOR COMPACT DISC SAA703

The circuit incorporates two identical filters (one per channel). Each is a finite impulse response, linear phase transversal filter. The filter length is 96 bits with 16-bit data words and 12-bit coefficients. The composition of each filter is as follows:

serial-to-parallel input shift register;
sixteen 24-bit shift registers for data storage;
96 x 12-bit coefficient ROM;
12 x 16-bit array multiplier;
28-bit accumulator;
parallel-to-serial output shift register.

Overflow protection is incorporated in the filters so that, in the unlikely event of accumulator overflow, the output limits cleanly. Overflow only occurs if the input samples continuously reverse sign coincidently with the coefficients, so that the products of the two entered into the accumulator are continually of the same sign.

The data inputs may run asynchronously with the master clock (CLOX) provided that the data inputs are always complete before the rising edge of the 44,1 kHz input strobe (STR1). A 176,4 kHz output strobe (LAT) is provided, the rising edge of which follows the completion of the serial output data stream. This strobe pulse is timed to be used to gate the master clock (CLOX) if required.

The input OS provides selection of −3% d.c. offset or no offset of the data output voltage level. The format of the output data is selected via the input $\overline{OB}$ to be in offset binary or two's complement form.

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	OS	Offset select input. When connected to V_{DD1}, the data output has a fixed d.c. offset of −3%. When connected to V_{SS}, the data output has no offset.
3	DLFD	Left channel data output. The data is 14-bit serial with most-significant bit first and is valid on the falling edge of the output clock ($\overline{CLFD}$).
6	$\overline{CLFD}$	Data clock output. Typical frequency = 4,2336 MHz (= CLOX). The falling edge of this clock defines output data valid.
7	LAT	Strobe output at 176,4 kHz. The rising edge of this pulse indicates that the output of a 14-bit data word is complete.
10	DRFD	Right channel data output (see DLFD).
11	$\overline{OB}$	Offset binary/two's complement select input. When connected to V_{SS}, the output data is coded in offset binary. When connected to V_{DD1}, the output data is coded in two's complement.
12	V_{SS}	Ground (0 V).
13	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
14	TEST1	Test output; not used in normal operation.
15	TEST2	Test input; in normal operation this pin should be connected to V_{SS} or V_{DD1}.
16	TEST3	Test input; in normal operation this pin should be connected to V_{SS} or V_{DD1}.
17	DRCF	Right channel data input. Data should be 16-bit serial with most-significant-bit first and in offset binary code. It is valid on the falling edge of the input data clock ($\overline{CLCF}$).
18	$\overline{CLCF}$	Input data clock. The falling edge of this clock defines input data valid.
19	CLOX	Master clock input. Runs continuously at a typical frequency of 4,2336 MHz.
20	DLCF	Left channel data input (see DRCF).

FILTER CIRCUIT FOR COMPACT DISC

FUNCTIONAL DESCRIPTION (continued)

pin no.	mnemonic	description
21	STR1	Strobe input at 44,1 kHz. The internal timing chain of the SAA7030 is synchronized by the rising edge of STR1 which must be synchronous with CLOX within the tolerance specified in CHARACTERISTICS. The rising edge should follow the completion of the input data stream.
22	TEST4	Test input; in normal operation this pin should be connected to V_{DD1}.
23	TEST5	Test input; in normal operation this pin should be connected to V_{DD1}.
24	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

Pins 4, 5, 8 and 9 have no internal connection.

3

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

FILTER CIRCUIT FOR COMPACT DISC — SAA703

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); V_{SS} = 0 V

Supply voltage 1 range (pin 24)	V_{DD1}	−0,3 to + 7,5	V
Supply voltage 2 range (pin 13)	V_{DD2}	−0,3 to + 15	V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3	V
Input voltage range	V_I	−0,3 to + 7,5	V
Output voltage range	V_O	−0,3 to + 7,5	V
Output current	I_O	max. 10	mA
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 24)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 13)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 24)	I_{DD1}	50	120	240	mA
Supply current 2 (pin 13)	I_{DD2}	3,5	8,0	15,0	mA
Back bias supply current (pin 1) at $V_{DD1} \leqslant 5,5$ V; $V_{DD2} \leqslant 13,2$ V	$-I_{BB}$	–	–	500	µA
Inputs					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at T_{amb} = 25 °C; V_I = −0,3 to + 6,5 V	$\pm I_I$	–	–	1	µA
Input capacitance	C_I	–	–	7	pF
Outputs (note 1)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	−0,3	–	+ 0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	50	150	pF
Input CLOX					
Operating frequency	f_{IX}	1,0	4,23	4,5	MHz
Input clock LOW	t_{IXL}	25	–	–	% of t_{IXP}
Input clock HIGH	t_{IXH}	25	–	–	% of t_{IXP}

FILTER CIRCUIT FOR COMPACT DISC

CHARACTERISTICS (continued)

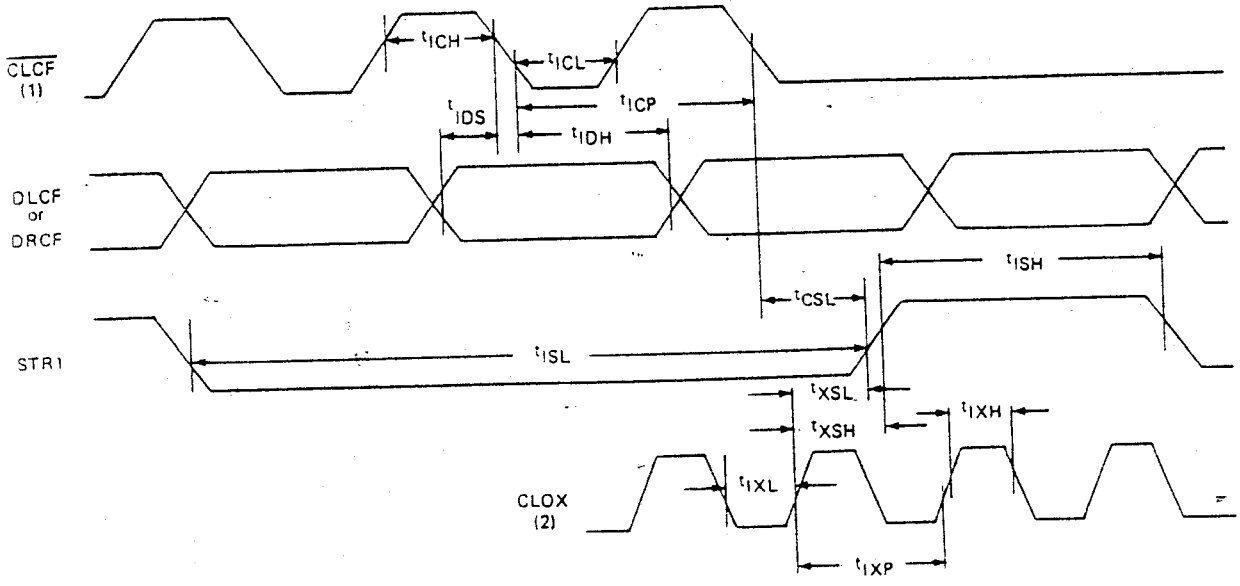
parameter	symbol	min.	typ.	max.	unit
Inputs $\overline{CLCF}$, DLCF, DRCF, STR1					
$\overline{CLCF}$ frequency	f_{IC}	0,1	2,12	4,50	MHz
$\overline{CLCF}$ LOW time	t_{ICL}	75	–	–	ns
$\overline{CLCF}$ HIGH time	t_{ICH}	75	–	–	ns
DLCF/DRCF to $\overline{CLCF}$ set-up time	t_{IDS}	25	–	–	ns
$\overline{CLCF}$ to DLCF/DRCF hold time	t_{IDH}	75	–	–	ns
$\overline{CLCF}$ LOW to STR1 time	t_{CSL}	0	–	–	ns
STR1 LOW time	t_{ISL}	4	–	–	CLOX cycles
STR1 HIGH time	t_{ISH}	1	–	–	CLOX cycles
CLOX to STR1 rising	t_{XSL}	−5	–	–	ns
CLOX to STR1 HIGH	t_{XSH}	–	–	55	ns
Outputs $\overline{CLFD}$, DRFD, DLFD, LAT (notes 2 and 3)					
Output rise time (except LAT)	t_{OR}	–	10	30	ns
Output fall time (except LAT)	t_{OF}	–	8	15	ns
Output rise time (LAT only)	t_{LR}	–	7	15	ns
Output fall time (LAT only)	t_{LF}	–	6	10	ns
$\overline{CLFD}$ HIGH time	t_{OCH}	40	75	–	ns
$\overline{CLFD}$ LOW time	t_{OCL}	40	105	–	ns
DRFD/DLFD to $\overline{CLFD}$ set-up time	t_{ODS}	20	70	–	ns
$\overline{CLFD}$ to DRFD/DLFD hold time	t_{ODH}	50	120	–	ns
$\overline{CLFD}$ LOW prior to LAT rising	t_{CLD}	100	350	–	ns
CLOX to LAT starting to change (note 4)	t_{XLS}	0	30	–	ns
CLOX to LAT reaching final value	t_{XLF}	0	80	–	ns
$\overline{CLFD}$ LOW to rising edge of CLOX with rising edge to STR1	t_{XCL}	50	400	–	ns
LAT HIGH time	t_{LH}	–	1	–	CLOX cycle

NOTES TO THE CHARACTERISTICS

1. All outputs are protected against short-circuit to V_{SS} and V_{DD1}. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
2. Output loading C_L = 50 pF.
3. Reference levels are 0,8 and 2 V.
4. Rising edge of LAT occurs in the first CLOX LOW period following the rising edge to STR1 and then recurs at every 24th CLOX cycle.

FILTER CIRCUIT FOR COMPACT DISC

Fig. 3 Typical input and output waveforms (for illustration only).



(1) $\overline{\text{CLCF}}$ frequency (f_{IC}) = $1/t_{ICP}$. The trailing edge of $\overline{\text{CLCF}}$ must occur 16 times between consecutive rising edges of STR1.

(2) CLOX frequency (f_{IX}) = $1/t_{IXP}$.

Fig. 4 Input waveform timing; reference levels are 0,8 and 2 V.

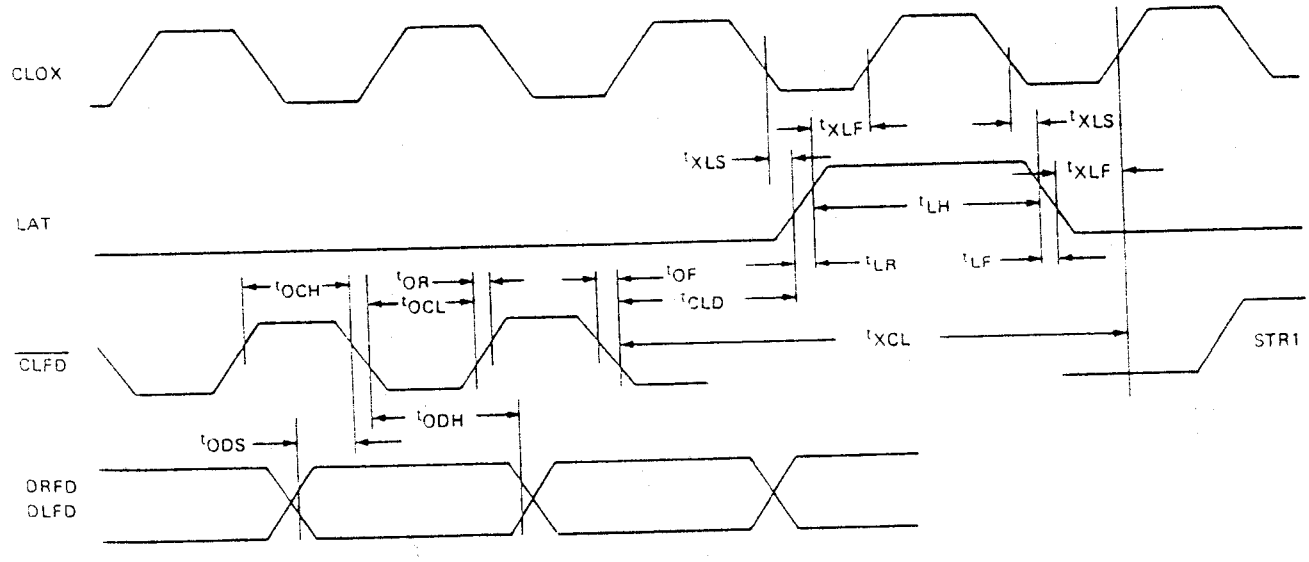


Fig. 5 Output waveform timing: reference levels are 0,8 and 2 V; output loading = 50 pF.